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# EDN®

VOICE OF THE ENGINEER

OCT 26
Issue 22/2006
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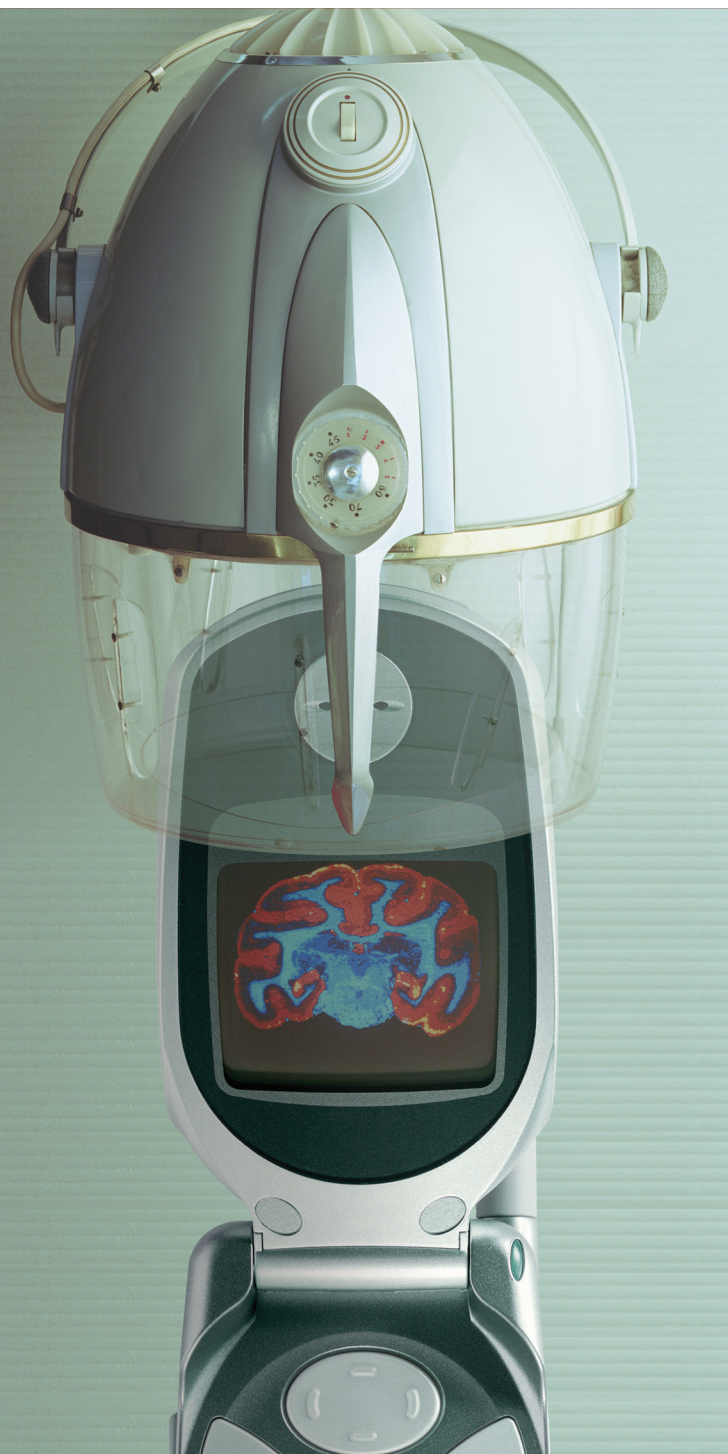
HANDS-ON PROJECT

# MOBILE MAKEOVER

Page 54



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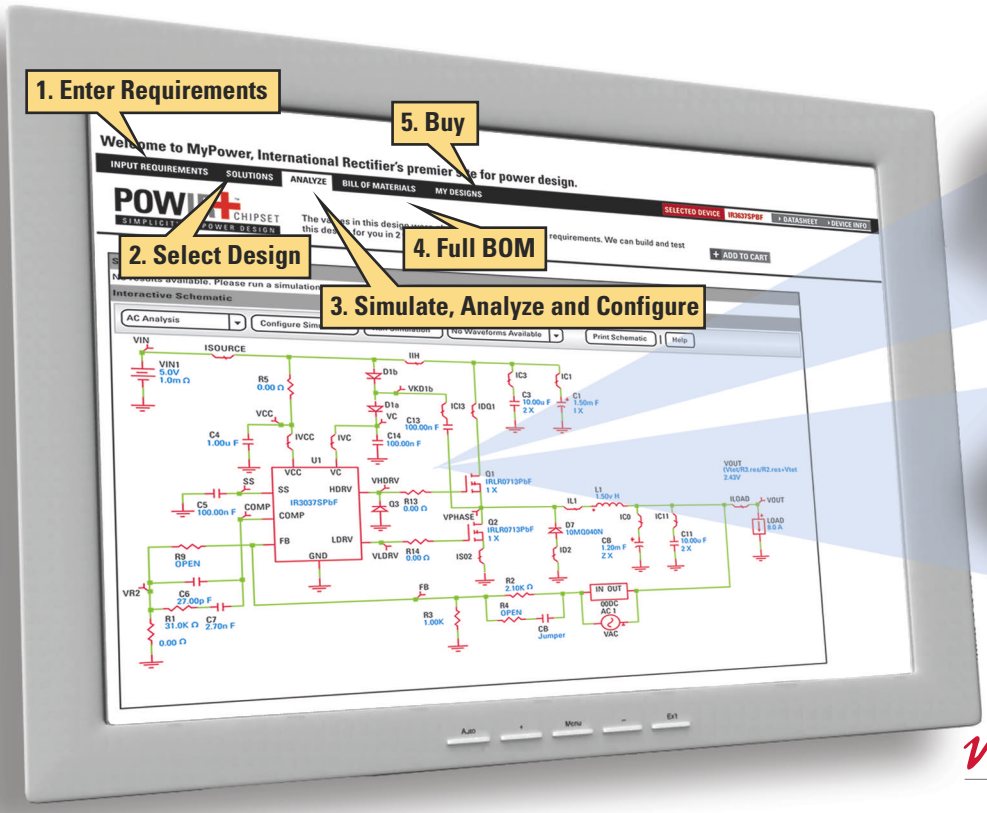
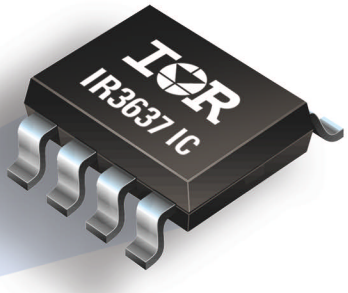
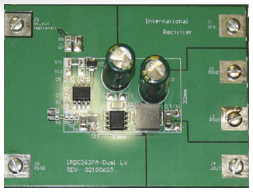




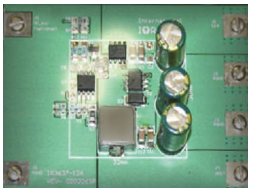
**myPOWER online design**

**IRPP3637-06A**



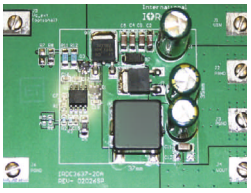
**5V$_{in}$ / 1.25V$_{out}$**
**@ 6A & 600kHz ~1.0in$^2$**

**IRPP3637-12A**



**12V$_{in}$ / 1.8V$_{out}$**
**@ 12A & 400kHz ~1.5in$^2$**

**IRPP3637-18A**



**12V$_{in}$ / 3.3V$_{out}$**
**@ 18A & 400kHz~2.0in$^2$**

| Part Number | Input Voltage | Output Voltage | Output Current | Swithcing Frequency | Power Semi BOM | Delivery Time | Comments |
|---|---|---|---|---|---|---|---|
| IRPP3637-06A | 5V | 1.25V | 6A | 600kHz | IR3637AS, IRF8910 | 24-48Hrs | Standard Ref Design<br>Fixed BOM |
| IRPP3637-12A | 12V | 1.8V | 12A | 400kHz | IR3637S, IRF7823, IRF7832Z | | |
| IRPP3637-18A | 12V | 3.3V | 18A | 400kHz | IR3637S, IRLR8713, IRLR7843 | | |
| IRPP3637-06AC | 3.0V to 13.2V | 0.8V to 5.0V | Up to 6A | 400kHz or 600kHz | Various | 1-2 Wks | Customizable Ref Design<br>BOM configurable on-line.<br>Operating range defined is NOT possible with one BOM |
| IRPP3637-12AC | | | Up to 12A | | Various | | |
| IRPP3637-18AC | | | Up to 18A | | Various | | |

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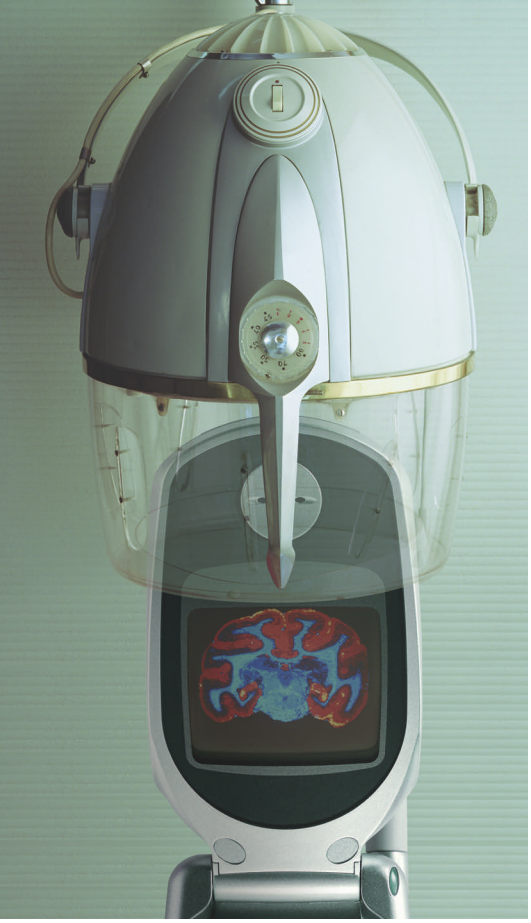

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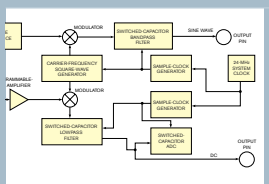
50 years

# contents

10.26.06



# DESIGNIDEAS

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Dilbert 26




26

42

116

## DEPARTMENTS & COLUMNS



## PRODUCT ROUNDUP




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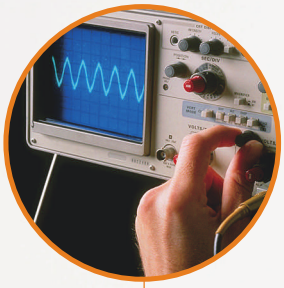

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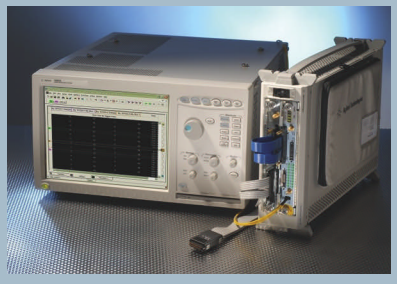

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Agilent Technologies has announced what it calls the industry's first complete and integrated ×1 through ×16 protocol analyzer and exerciser system for 5-Gbps PCIe (PCI Express) 2.0, which doubles the 1.x protocol's speed.
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**Gain-selectable amps compensate for bandwidth roll-off**
Microchip's new MCP6G01 and MCP6G02 series of amplifiers uses one pin to select a gain of one, 10, or 50 at 1 MHz, 350 kHz, and 300 kHz, respectively.
→ www.edn.com/article/CA6367508

**Light version of IP interconnects hardware blocks**
While it has been busy licensing its wares into some of the most influential platform designs in the industry, including Texas Instruments' (www.ti.com) OMAP (Open Multimedia Applications Platform) architecture, Sonics has been in an uphill battle to define the concept of interconnect IP (intellectual property).
→ www.edn.com/article/CA6370309

**Our man at the Intel Developer Forum**
Here's a roundup of posts that Senior Technical Editor Brian Dipert filed in his blog, Brian's Brain, while attending the Intel Developer Forum.
→ www.edn.com/article/CA6376152

## READERS' CHOICE

*A selection of recent articles receiving high traffic on www.edn.com.*

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→ www.edn.com/article/CA6368459

**Spice simulator offers speed, capacity increase over competitors**
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**Paradoxically, RF integration may be SiGe's best friend**
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**Making waves: Eight years later, details still matter**
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**Abracadabra: Making system interconnect disappear with FPGAs**
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## INNOVATION AWARDS

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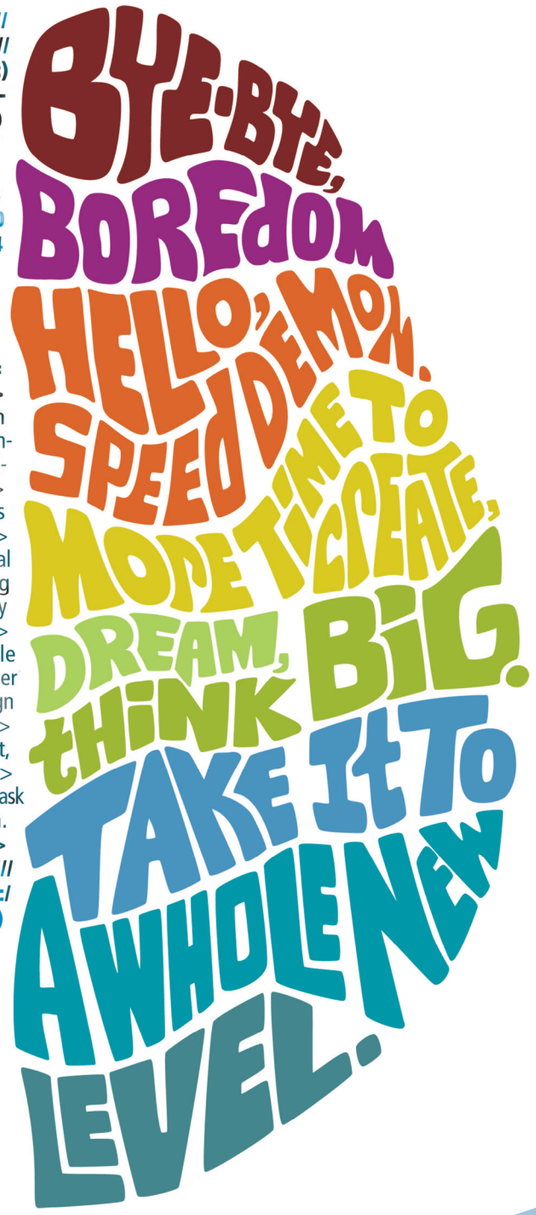


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BY MAURY WRIGHT, EDITOR IN CHIEF

# Cellular radios: Not just for phones anymore

The most compelling products and presentations at the Demo Fall conference (Sept 26 to 27, www.demo.com) in San Diego, CA, all centered on mobile connectivity. Perhaps the focus shouldn't have surprised me, because the name of the autumn version of the conference used to be Demo Mobile. But "mobile," in this case, was a bit different. The conference featured its share of handsets with cameras and other sensors enhancing the basic phone functions. The most compelling concepts, however, used an integrated cellular radio as just another enabling component.

The best product pitch came from Dash Navigation (www.dash.net) in the first session. Dash introduced an automotive-GPS (global-positioning-system) product that looks like many of the others on the market. But Dash integrates a cellular radio in its device. The cellular connection allows real-time communications in both directions. That scenario means that you might actually find the restaurant or theater that wasn't in your latest data update for a conventional GPS.

Of more importance, the cellular connection allows Dash to send you real-time traffic updates and routing. Dash takes traffic-flow information that is available from service providers in major cities and real-time data from other Dash customers and provides real-time ETA data and alternative routes. The company didn't release prices but claims that hardware prices will be competitive with other auto-GPS systems. Dash, will, however, charge a monthly service fee as well. But Dash's are the first GPS products to offer real value every time you get in the car: Traffic flow is much more important than navigation for most of us, especially in our local areas.

Paul Jacobs, Qualcomm's chief executive officer, also addressed embedded-cellular applications in addition to the latest phone technology. I had never heard a Qualcomm executive speak without trying to make the case that the phone would usurp all other portable applications. Jacobs, however, went into detail on consumer products that might have an integrated cellular radio playing second fiddle.

Jacobs cited a portable game machine as an example, pointing out that an embedded radio would potentially enable multiplayer gaming, in-game advertising, or "smack talk" between players. And it was refreshing to hear Jacobs acknowledge that consumers wouldn't be expected to have separate subscriptions for all such devices that might have a cellular radio. "The industry now is working through the idea: How do you have a subscription and then transfer it among your various devices?" he said. "It's the device that you have with you, or maybe a couple of devices, that you'll have the subscription on."

The applications go way beyond entertainment. Jacobs cited a cellular-enabled glucometer as an example. Parents of a diabetic kid or a doctor managing a critically ill patient might find such a device invaluable. Jacobs also claimed that heart monitors have integrated cellular radios.

Of course, Jacobs did cite advances in phone-centric devices, as well. He showed a phone that is shipping in Asia that integrates a 4-Gbyte disk drive and suggested that phones would serve as DVRs (digital-video recorders). And, no, you don't have to watch the programming on the small screen. Jacobs claimed that high-end phones will have video out to drive large displays, and, currently, the phones sport better graphics than those in the original Sony PlayStation. He also asserted that the phone-to-flat-panel link may ultimately come by means of a standard, such as Wireless USB.

What does this scenario mean for designers? Start thinking about how wireless-WAN connectivity can affordably enhance your next product.EDN

*Contact me at mgwright@edn.com.*

## MOORE'S LAW OR MURPHY'S LAW?

**In our last issue, we formally celebrated our 50th anniversary and mailed subscribers what we think is a cool poster listing industry milestones. I expected disagreement over our milestone choices, and, indeed, these comments are flowing in. But I didn't intend to have to admit an embarrassing error in the poster: The photo that we associated with Moore's Law is *not* of Gordon Moore. The gentleman in the photo is Nick Holonyak, an engineering professor from the University of Illinois who has many accomplishments to his credit, including a National Medal of Technology for his work with LEDs. We also, somehow, listed 1971 as the date for Moore's Law, although it really dates back to 1965. We should have caught both errors. We apologize for the mistakes to all readers and to Gordon Moore and Nick Holonyak.**


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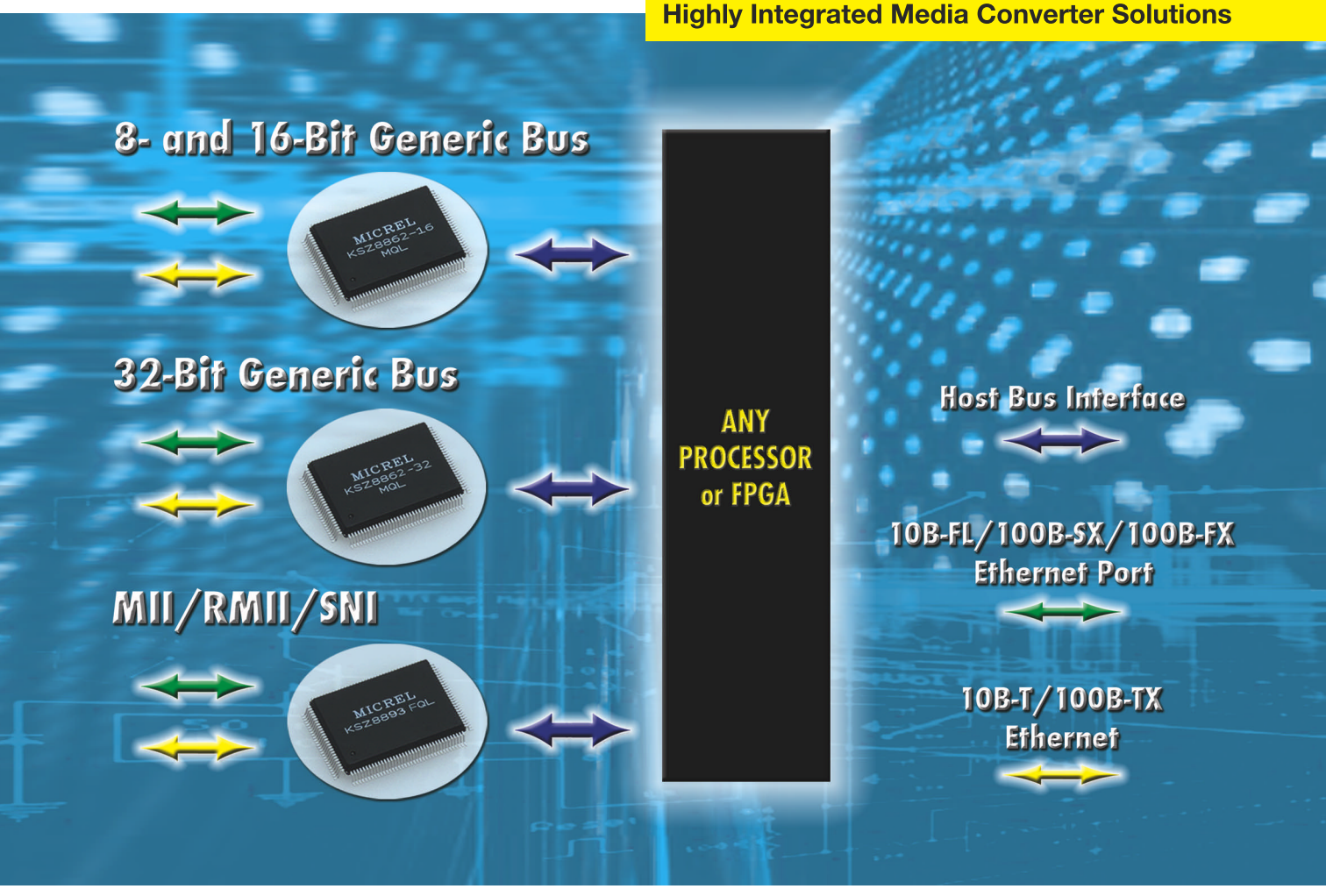


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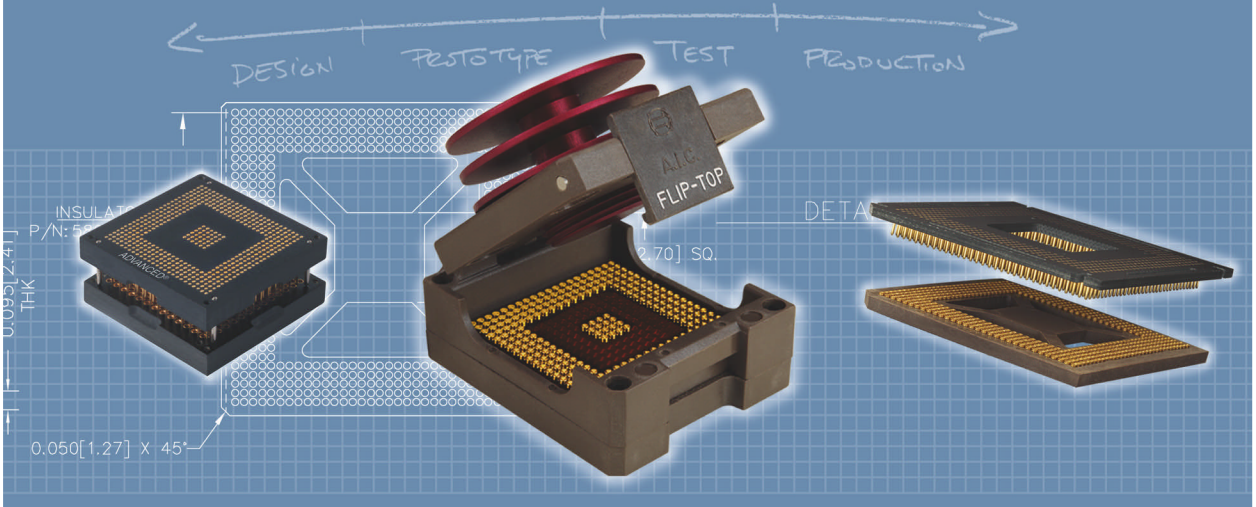


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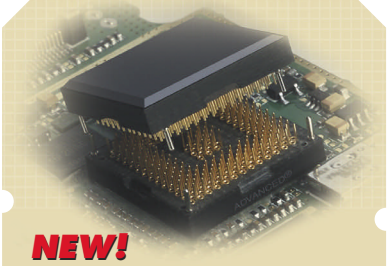

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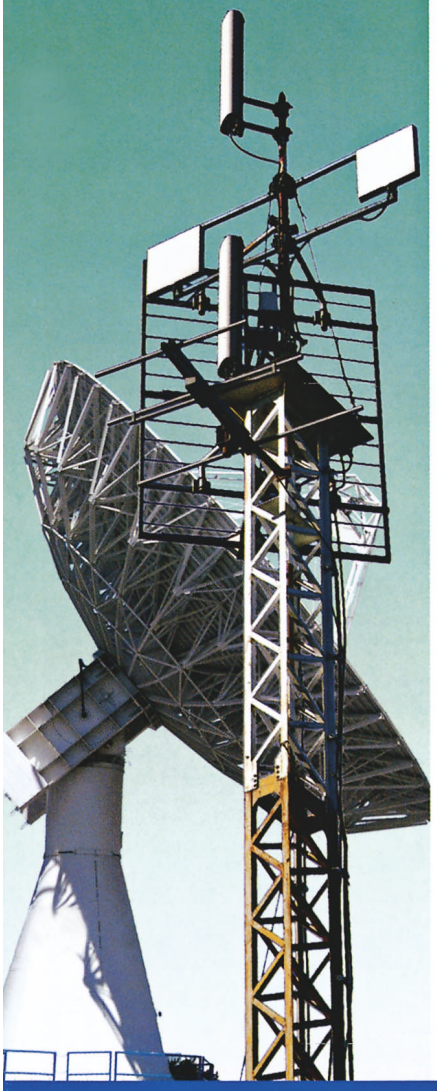
*Tips, tricks, and techniques from the analog signal-path experts*

No. 107



## Delay Calibration of Signal Path Interconnect

### In Remote Radio Head (RRH) Basestations and Other Applications

*— By Dave Lewis, Interface Applications Manager*

Calibrating delays through a signal path is growing in importance as systems become faster and more parallel. Often, the system needs to know the delay from the central processing unit to remote A/D and D/A modules and then be able to compensate for any delay variations between one signal path and the others. Example applications where delay calibration may be useful include wireless basestations, radar, satellite, test equipment, medical imaging, particle accelerator equipment, and other high-performance applications. This issue of the ***Signal Path Designer*** will focus on basestations as an example, to see how National's SCAN25100 serializer/deserializer (SerDes) performs precision delay calibration measurement.

### Basestations

There is a growing trend in wireless basestations to move the radio electronics from the basestation to the antennas, increasing radio efficiency, deployment flexibility, and coverage while consolidating DSP and backhaul resources for lower CAPEX and OPEX. These Remote Radio Heads (RRHs), however, can be a challenge to synchronize back to the central basestation "hotel." A second challenge is calibrating every delay path from each antenna to the basestation. This article will examine these two timing challenges in more detail.

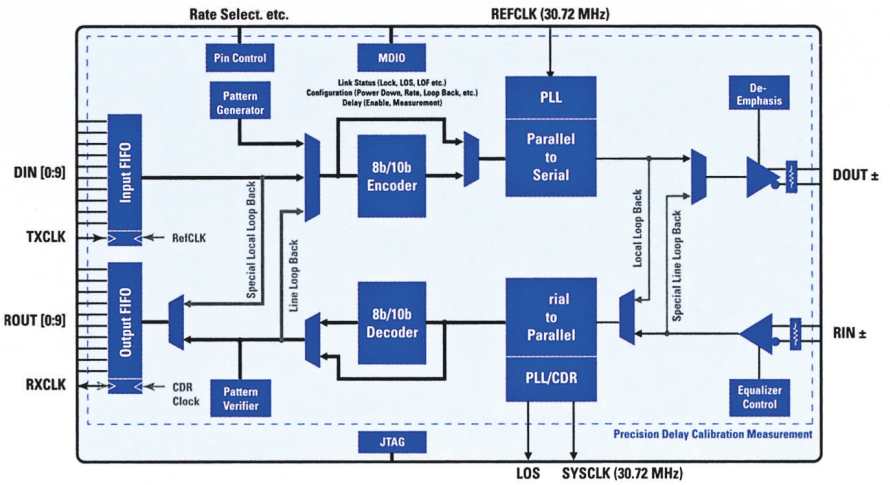



**Figure 1. SCAN25100 Next-Generation CPRI SerDes Block Diagram**

**NEXT ISSUE:**
**Current-Loop Transmitter**

National Semiconductor
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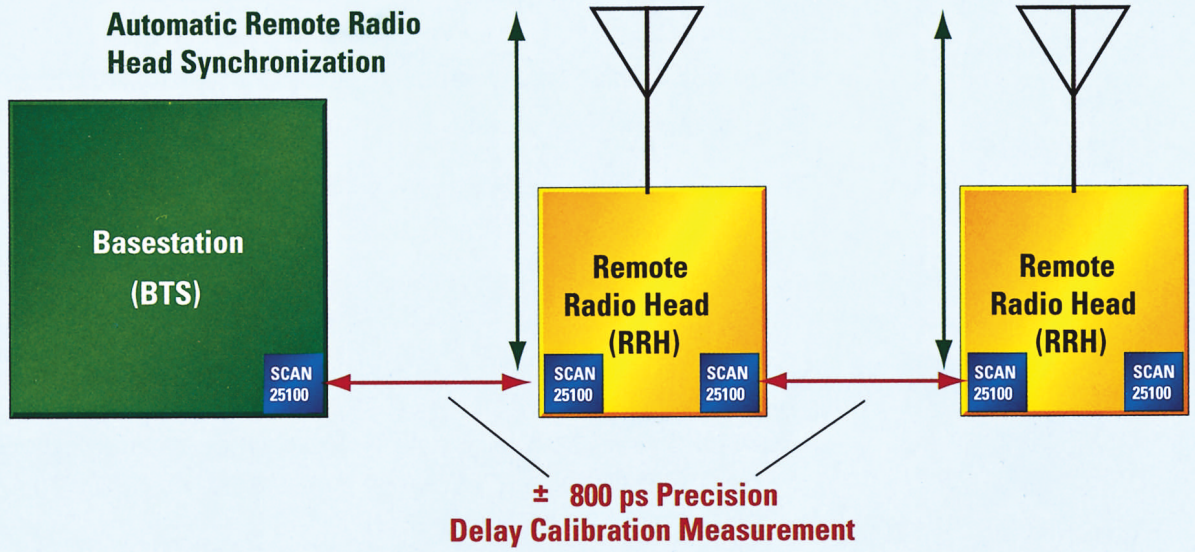
# Interface and ADC Solutions for Next-Generation Basestations

## SerDes with Integrated 30.72 MHz Clocking and Precision Delay Calibration Measurement



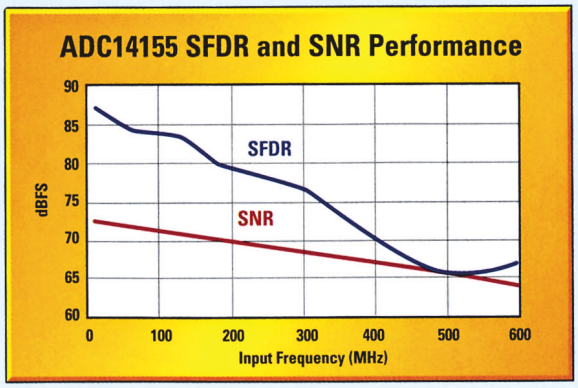

### SCAN25100 Features

- 2457.6, 1228.8, and 614.4 Mbps operation
- Exceeds both LV and HV CPRI v2.0 physical interface requirements
- Superior jitter tolerance and link performance
- Precision delay calibration circuitry measures delay with ± 800 ps accuracy
- Deterministic chip latency
- Automatic remote radio head synchronization
- Receiver locks without a reference clock
- Low phase noise 30.72 MHz recovered clock output
- Serializer output jitter independent of $Ref_{CLK}$
- Industrial –40 to +85°C temperature range
- Available in TQFP-100 packaging

## 1.1 GHz Bandwidth 14-bit, 155 MSPS ADC Enables High IF Sampling

### ADC14155 Features

- 1.1 GHz full power bandwidth
- Digitize IFs as high as 450 MHz
- Dual 3.3V and 1.8V supplies for low power consumption
- Duty cycle stabilizer
- Power down mode
- Straight binary or 2's compliment data format
- Internal precision 1.0V reference
- Data ready output clock
- Single or differential clock modes
- Available in LLP-48 packaging

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# Delay Calibration of Signal Path Interconnect

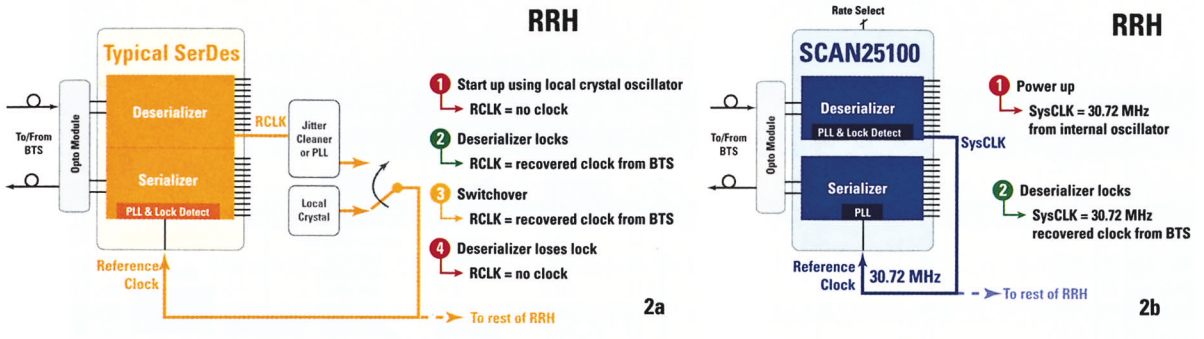



**Figure 2a and 2b. RRH Synchronization with Typical SerDes (a), with National's SCAN25100 (b)**

## RRH Synchronization

During initialization, the system must synchronize the entire network of remote radio heads to the basestation hotel even though the basestation (BTS) and RRHs are often separated by large distances over a serial fiber links. All data, control, and timing is carried by these serial streams—there is no high frequency clock sent in parallel—so each RRH must extract all timing information from the serial link. The RRH first starts up based on a local, on-board clock source. In this mode, it is free running and is not synchronized to the BTS. To synchronize to the BTS, the RRH must transition to its SerDes recovered clock once the SerDes is locked to incoming stream from the BTS. This clock switchover can cause many SerDes devices to lose lock because they use the reference clock to determine if the deserializer still locked. During the clock switch, the deserializer sees a phase and frequency change on reference clock and may decide it is no longer locked *(Figure 2a)*, reverting back to lock acquisition mode. This issue may not occur under all conditions, so it raises reliability concerns in the field.

National's SCAN25100 *(Figure 1)* incorporates separate, independent transmit and receive Phase Lock Loops (PLLs) and on-chip oscillator, enabling the deserializer to acquire lock without a reference clock. It seamlessly automates RRH synchronization through a special clock output called SysCLK. SysCLK reflects the SCAN25100 on-chip oscillator during start up to get the RRH logic up and running, but then transitions to the recovered clock once the deserializer locks to the incoming serial stream *(Figure 2b)*. SysCLK gracefully transitions from on-chip oscillator to recovered clock in order to allow downstream components to track this slight change in frequency. Since SysCLK is a low-noise output, it can be fed directly back to RefCLK in single-hop RRH applications, saving jitter-cleaning cost and complexity.

*Figure 1* shows the SCAN25100 has four clocks. The TxCLK and RxCLK are FIFO logic strobes for the parallel bus data timing and don't play a role in serializing or deserializing data. RefCLK, on the other hand, is used by the serializer to serialize data and should be a low jitter clock to minimize jitter on the serialized data stream. Finally, SysCLK reflects the internal on-chip oscillator before deserializer lock and then mirrors the recovered clock from the BTS data stream after deserializer lock. During this frequency transition, TxCLK should be held static high or low to prevent over- or under- flow of the parallel bus FIFO as shown in the typical start-up flow diagram in *Figure 3.*

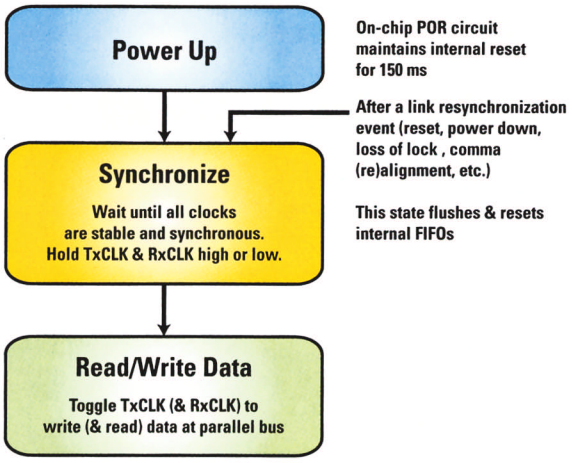
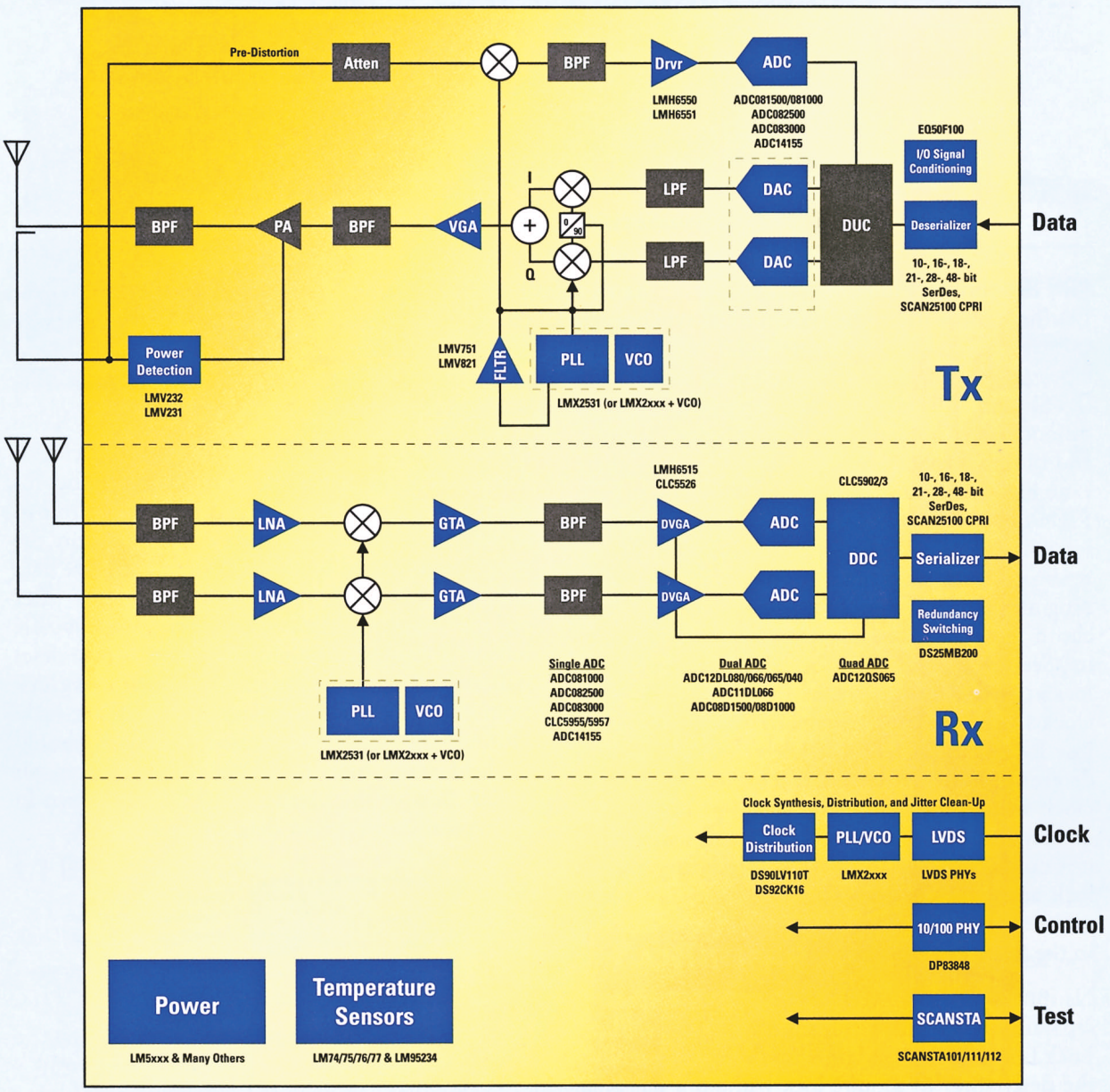



**Figure 3. SCAN25100 RRH Synchronization Start-Up Flow**

# Solutions for Wireless Infrastructure

## Typical Radio Diagram

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# Select Products

## High-Speed A/D Converters

| Product ID | Resolution | Max Speed (MSPS) | Supply Voltage | Power (mW) | SFDR (dB) | THD (dB) | ENOB (bit) | SNR (dB) | Packaging |
|---|---|---|---|---|---|---|---|---|---|
| **14-bit ADCs** | | | | | | | | | |
| ADC14L040 | 14-bit | 40 | 3.3 | 236 | 90 | 87 | 11.9 | 73 | LQFP-32 |
| ADC14155 | 14 bit | 155 | 3.3 | 980 | 84 | -81 | 11.5 | 71 | LLP-48 |
| **8-bit ADCs** | | | | | | | | | |
| ADC081000 | 8-bit | 1000 | 1.9 | 1450 | 59 | -57 | 7.5 | 48 | LQFP-128 exp pad |
| ADC081500 | 8-bit | 1500 | 1.9 | 1200 | 56 | -54.5 | 7.4 | 47 | LQFP-128 exp pad |
| ADC082500* | 8-bit | 2500 | 1.9 | 1750 | 57.5 | -55 | 7.25 | 45.6 | LQFP-128 exp pad |
| ADC083000* | 8-bit | 3000 | 1.9 | 1800 | 57.5 | -55 | 7.25 | 45.6 | LQFP-128 exp pad |
| ADC08D1000 | 8-bit dual | 2000 | 1.9 | 1600 | 55 | -55 | 7.4 | 47 | LQFP-128 exp pad |
| ADC08D1500 | 8-bit dual | 3000 | 1.9 | 1800 | 56 | -54.5 | 7.4 | 47 | LQFP-128 exp pad |
| ADC14C105* | 14-bit | 105 | 3.3 | 400 | 86 | 82 | 11.7 | 72.5 | LLP-32 |

## 2/2.5G Digital Down Converter (DDC)

| Product ID | Description |
|---|---|
| CLC5903 | 14-bit input resolution, 78 MSPS DDC with AGC control and 1.8V core supply voltage.<br>Very low 290 mW power consumption. SFDR is 100 dB, SNR is 127 dB, and tuning resolution is 0.02 Hz. |

## Precision Amplifiers

| Product ID | Description | $I_{cc}$/Ch (mA) | $V_{os}$ (mV) | GBW (MHz) | Noise (nV/$\sqrt{Hz}$) | Packaging |
|---|---|---|---|---|---|---|
| LMP7701/2/4 | Precision single/dual/quad | 0.7 | 0.2 | 2.5 | 9 | SOT23-5, MSOP-14, TSSOP-14 |
| LMP7711/12 | Precision single/dual | 1.15 | 0.15 | 17 | 5.8 | SOT23-6, MSOP-10 |
| LM6211 | Low noise 5 to 24V single with CMOS input | 1.05 | 2.5 | 20 | 5.5 | SOT23-5 |

## High-Speed Amplifiers

| Product ID | Type | Slew Rate (V/µs, $A_V$=1) | Small Signal Bandwidth (MHz, $A_V$=1) | $I_{cc}$ (mA/ch) | 2nd/3rd HD ($R_L$ = 100Ω) | Voltage Noise (nV/$\sqrt{Hz}$) | Packaging |
|---|---|---|---|---|---|---|---|
| LMH6550 | Single differential I/O amplifier | 3000 | 400 | 20 | -78/-88 at 20 MHz | 6 | SOIC-8, MSOP-8 |
| LMH6551 | Single differential I/O amplifier | 2400 | 370 | 12.5 | -94/-96 at 5 MHz | 6 | SOIC-8, MSOP-8 |
| LMH6702 | Single, op amp | 3100 | 1.76 GHz | 12.5 | -63/-72 at 60 MHz | 1.8 | SOT23-5, SOIC-8 |
| LMH6703 | Single, op amp | 4500 | 1.26 GHz | 11 | -69/-90 at 20 MHz | 2.3 | SOT23-5, SOIC-8 |
| CLC5526 | Digitally controlled variable gain amplifier | — | 350 | 48.0 | -67/-71 at 150 MHz | 2.2 | SSOP-20 |

## RF Detectors

| Product ID | Application | Detector | Channel | Range | Packaging |
|---|---|---|---|---|---|
| LMV221* | 3G, WCDMA, CDMA, UMTS, TD-SCDMA | Log amp | 1 | 40 dB, 3.5 GHz | LLP-6 |
| LMV232 | 3G, WCDMA, UMTS, TD-SCDMA | Mean square | 2 | 20 dB, 2.2 GHz | Micro SMD |

## Interface

| Product ID | Mux Ratio | Function | #Ser | #Des | Clock Speed (MHz) | Max Rate/Ch (Mbps) | Max Throughput (Mbps) | Temperature | Packaging | Eval Kit |
|---|---|---|---|---|---|---|---|---|---|---|
| **8b/10b CPRI Basestation SerDes** | | | | | | | | | | |
| SCAN12100 | 8:1 | SerDes | 1 | 1 | 30.72 | 614.4, 1228.8 | | -40 to +85°C | TQFP-100 | SCAN25100EVK |
| SCAN25100 | 8:1 | SerDes | 1 | 1 | 30.72 | 614.4, 1228.8, 2457.6 | | -40 to +85°C | TQFP-100 | SCAN25100EVK |

| Product ID | Function | In-puts | Out-puts | Muxing Options | Input Compatibility | Output | Pre-emphasis (dB)[1] | Receive Equal-ization (dB) | Max Speed/ Ch (Mbps) | Packaging |
|---|---|---|---|---|---|---|---|---|---|---|
| **Buffers** | | | | | | | | | | |
| DS25BR400 | Quad CML buffer | 8 | 8 | Loopback | LVDS/LVPECL/CML | CML | 0/-3/-6/-9 | 0/5 | 2500 | LLP-60 |
| DS42BR400 | Quad CML buffer | 8 | 8 | Loopback | LVDS/LVPECL/CML | CML | 0/-3/-6/-9 | 0/5 | 4250 | LLP-60 |
| **Multiplexers and Mux-Buffers** | | | | | | | | | | |
| DS25MB200 | Dual 2:1/1:2 mux/buffer | 6 | 6 | 2:1/1:2, LB | LVDS/LVPECL/CML | CML | 0/-3/-6/-9 | 0/5 | 2500 | LLP-48 |
| DS40MB200 | Dual 2:1/1:2 mux/buffer | 6 | 6 | 2:1/1:2, LB | LVDS/LVPECL/CML | CML | 0/-3/-6/-9 | 0/5 | 4000 | LLP-48 |

* Preliminary product information

[1] CML devices in this column that feature de-emphasis show a negative dB

# Delay Calibration of Signal Path Interconnect

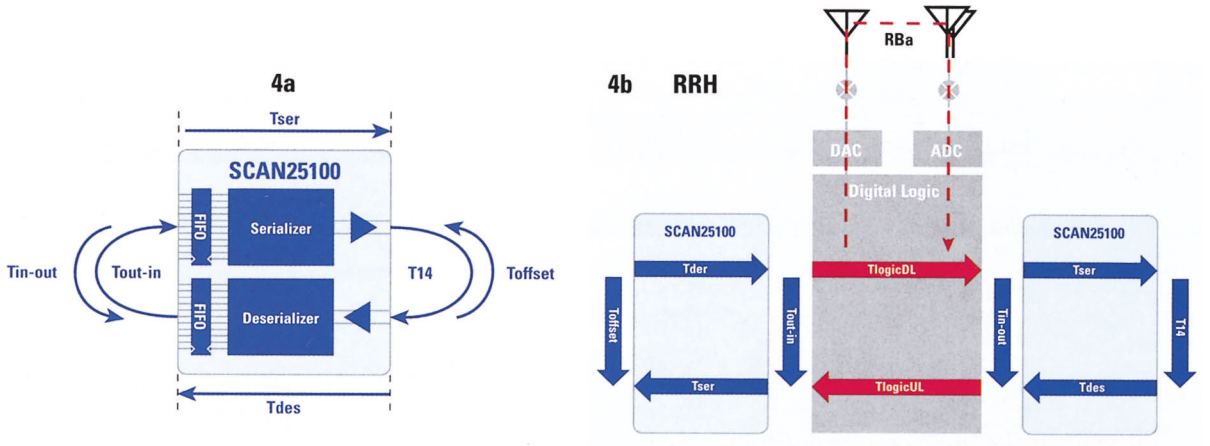


**Figure 4a and 4b. SCAN25100 Delay Calibration Measurement Operation (a), Results (b), Intra-RRH Delay Measurement Example**

## Delay Calibration

After the system powers up and the RRHs are frequency-locked to the BTS, the system must calibrate all delays between RRHs and the BTS to meet air-interface timing requirements. Delay measurement in basestations is usually accomplished using frame timing. For example, the CPRI basestation standard specifies that the delay between an RRH and a BTS is $(T14 - T_{OFFSET})/2$, where T14 is the delay between transmitting and receiving a hyperframe at the BTS and $T_{OFFSET}$ is the delay between receiving and transmitting a hyperframe at the RRH. Assuming the system is synchronous, hyperframes have fixed length and the RRH-BTS interconnect delay is equal in both directions (e.g. both optical fibers are in one bundle), the interconnect delay is just the difference in hyperframe arrival and departure times measured at each side of the link.

The SCAN25100 simplifies delay calibration by directly reporting T14 and $T_{OFFSET}$ delays as well as its own chip delay *(Figure 4a)*. In addition, the SCAN25100 also measures something National calls $T_{IN-OUT}$ and $T_{OUT-IN}$. These delays are just like T14 and $T_{OFFSET}$ but where T14 and $T_{OFFSET}$ are measured at the serial bus, $T_{IN-OUT}$ and $T_{OUT-IN}$ are measured at the parallel bus. That means the system can use $T_{IN-OUT}$ and $T_{OUT-IN}$ to measure digital logic delays, and with loop back, even delays in the analog RF signal path *(Figure 4b)*.

Delay measurement accuracy requirements for RRH systems are typically on the order of 10 ns, however in multi-hop RRH networks where RRHs are cascaded, delay measurement errors from each hop are additive and higher precision may be required. National's SCAN25100 guarantees T14 and $T_{OFFSET}$ accuracy to better than ± 800 ps while Tser, Tdes, $T_{IN-OUT}$, and $T_{OUT-IN}$ are accurate to better than ± 1.2 ns, allowing reliable and precise control over basestation system timing. All delay measurements are performed transparently (the data stream is not interrupted) on request as often as every 5 ms, letting the system track delay changes over the life of the system.

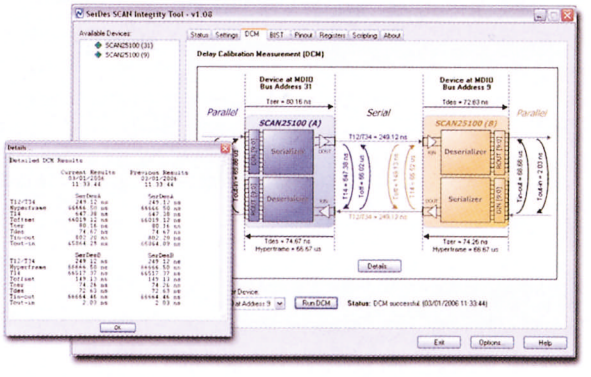

**Figure 5. SCAN25100 Evaluation Software Showing Delay Calibration Measurement Results**

## Measuring Light

Traditional basestation delays were typically calibrated using special test equipment and were not expected to change significantly over time. Distributed RRH networks, however, cover a wide area and BTS-RRH fiber interconnect delays may change significantly over temperature. For example, a temperature swing from -40° to +40°C on 15 km single mode fiber can result in a ≈37 ns delay shift *(Figure 6)*. This is probably enough to violate basestation timing requirements after just one hop.

| | | |
|---|---|---|
| Fiber Delay Variation | | 31 ps/°C/km |
| Temperature Range | x | 80°C (-40 to +40°C) |
| Fiber Length | x | 15 km |
| **Total Delay Change** | | **37.2 ns** |

**Figure 6. Single Mode Fiber Propagation Delay Change Due to 80°C Temperature Shift**

The delay measurement resolution or granularity of the SCAN25100 is ≈200 ps delay, enabling it to track small delay variations in RRH fiber links over temperature. To prove this, National conducted an experiment by placing a one kilometer spool of single mode fiber into a well-insulated box while slowly increasing the temperature from about 20°C to 45°C using a SCAN25100 to monitor fiber delay. Experiment results consistently demonstrated a 31 ps/°C/km coefficient *(Figure 7)* which closely agrees with investigations published by particle accelerator physicists.

## Conclusion

SCAN25100 automatic synchronization and precision delay calibration ease the design of distributed remote radio basestation systems. Having high delay calibration accuracy also opens the door to new parallel approaches to signal acquisition and processing. For example, in basestations SCAN25100 precision delay calibration measurement can enable wider remote antenna placement via independent RRH links, thereby increasing diversity. In the future, system designers may even coordinate clusters of multi-element antennas to reduce interference while increasing coverage and capacity. The SCAN25100 couldalso be employed similarly in non-basestation applications to match phase and frequency across multiple parallel signal acquisition or signal processing paths. ■

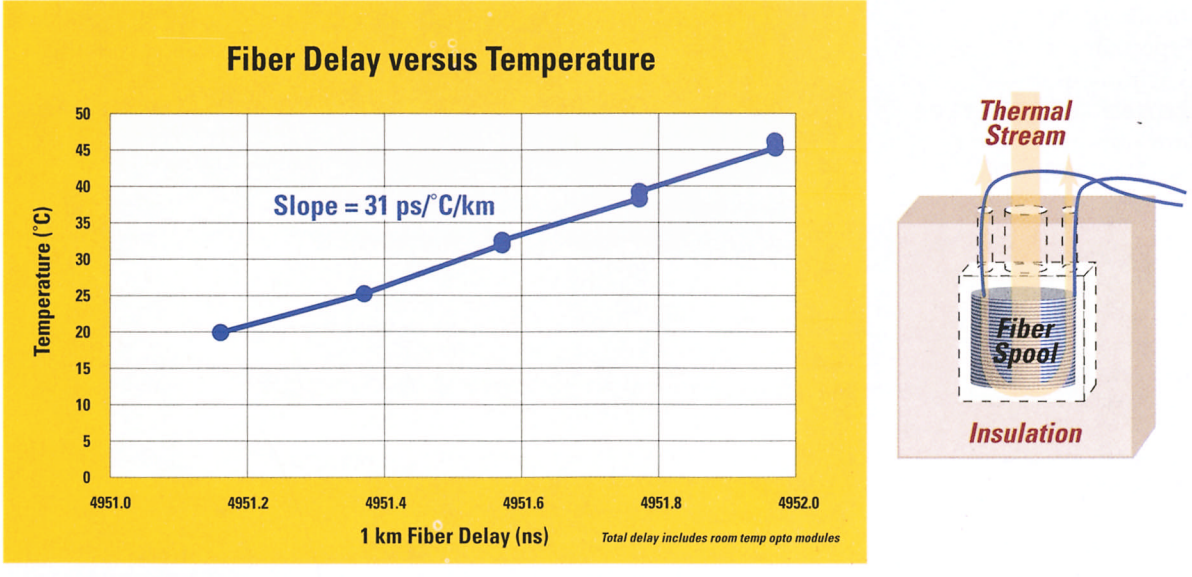


**Figure 7. Experiment results: Using the SCAN25100 to track fiber delay changes over temperature.**

# Design Tools

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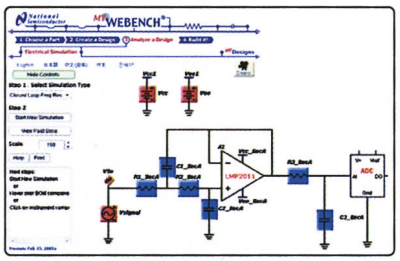


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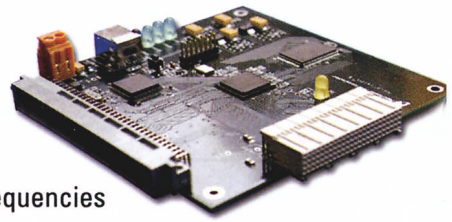

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# Waveform-viewer software works with four suppliers' DSOs

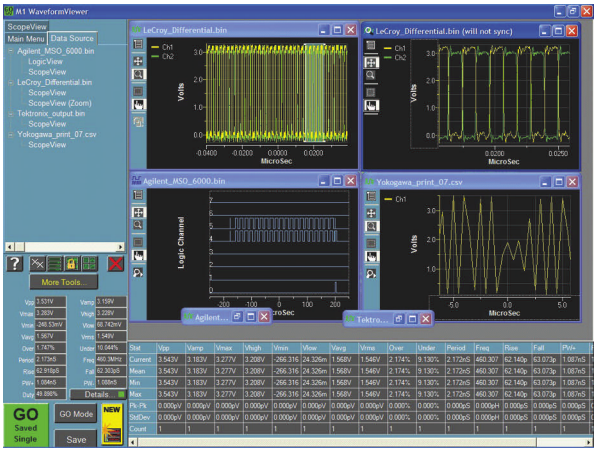
Many signal-integrity experts who measure jitter and other phenomena through scope-based measurements recognize the name Amherst Systems Associates (ASA), though the name is hardly a household word to other EEs. The company has, for many years, marketed the M1 package (now at revision level V4), which operates on data that scopes from the four major high-performance-scope manufacturers gather. Those manufacturers are Agilent (www.agilent.com), LeCroy (www.lecroy.com), Tektronix (www.tektronix.com), and Yokogawa (www.yokogawa.com). Some of these manufacturers offer M1 in addition to their own measurement packages, and some signal-integrity experts regard the package as the impartial arbiter when scopes from different manufacturers and sometimes even different models from the same manufacturer disagree on values they calculate from acquired data sets.

Now, ASA is offering what it calls the first low-cost viewer that works with data acquired from a long list of scopes—both real- and equivalent-time—from all four manufacturers. M1 WV (M1 Waveform Viewer), whose list price is $145, is currently available as a free download from ASA's Web site. ASA hopes that those who download the viewer will eventually purchase the complete M1 package, but the WV product functions fully as a viewer that can save waveform data from multiple scope models in a common format, greatly simplifying comparing data from different scopes. In addition, ASA neither limits nor plans to limit how long you can continue to use the viewer.

Greg Walz, product manager at the company, points out that, although all high-performance scopes can save waveform records as text files, because of subtle differences in the file formats, files from different scope models do not, in general, successfully load into different-model scopes. Moreover, because waveform records now usually encompass data that you can view satisfactorily only by scrolling through many screens, screen dumps in such standard graphics formats as TIF and PNG, though interchangeable among different scopes, do not contain sufficient data for most engineers' comparison and analysis purposes.

**—by Dan Strassberg**

▷**Amherst Systems Associates**, www.amherst-systems.com.




The M1 Waveform Viewer allows you to load and simultaneously display waveform records from multiple manufacturers' high-performance digital scopes.

## FROM THE VAULT

**"It's safe to assume that the billions of dollars of *tax money* needed for the SSC (Superconducting Super Collider) must come from other programs' budgets rather than from new tax revenues. So, it's time to decide whether the Super Collider is worth the price. If we must take money from existing and planned projects, let's consider refurbishing and rejuvenating college and university laboratories with it. The payoff would be quick."**

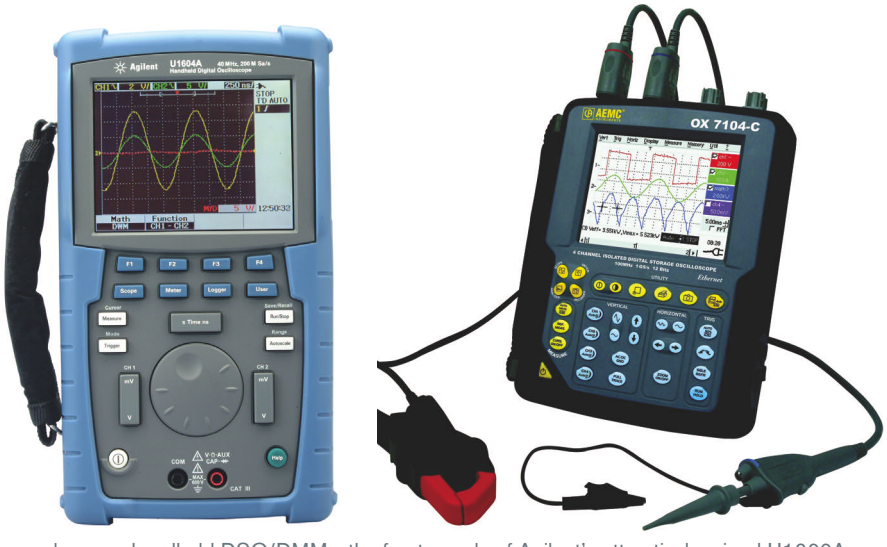
Jon Titus, former *EDN* editor in chief, *EDN*, Sept 1, 1988, pg 51.

# Two new suppliers broaden users' handheld-DSO choices

Although the list of handheld-DSO/DMM (digital-storage-oscilloscope/digital-multimeter) manufacturers includes at least three companies, most EEs are familiar with only Fluke Corp (www.fluke.com), whose ScopeMeter products are so widely distributed that many potential customers think of them as the *only* handheld scope/DMMs.

Now, Fluke and its competitors have competition from two more companies. Agilent has introduced two handheld scope/DMMs, and AEMC, which scope and multimeter manufacturers recognize as a leading OEM supplier of current probes and similar accessories, has announced a product that offers more channels than do the Agilent unit and some capabilities not present in previously announced handheld scope/DMMs.

Agilent's $1320 U1602A offers two 20-MHz-bandwidth-scope channels and a true-rms-responding (on ac measurements), 6000-count DMM. The $1650 U1604A's two scope channels each provide 40-MHz bandwidth. On both units, the maximum acquisition rate is 100M samples/sec with both channels in use or 200M samples/sec in interleaved mode. Both units offer 8-bit scope resolution, a 320×240-pixel, 4.5-in. color LCD, and the ability to perform waveform math; the U1604A also performs FFTs (fast-Fourier transforms). Both units ohmically isolate the scope inputs from the case and the ground terminal but not from each other.




Unusual among handheld DSO/DMMs, the front panels of Agilent's attractively priced U1600A series each sport a large rotary control (left). AEMC's OX 7104-CK provides four separately isolated 100-MHz-bandwidth-scope channels and four DMM channels as well as FFT and harmonic analyzers (right).

Many users will also applaud the rotary front-panel control, an unusual feature in handheld scopes.

AEMC's $3595 OX 7104-CK provides four 100-MHz-bandwdith-scope channels, each with 12-bit resolution and each ohmically isolated from the others, from the case, and from ground. Maximum sampling rate on each channel is 1G samples/sec in single-shot mode and 25G samples/sec in equivalent-time mode. Memory depth is 2.5k samples/channel. Although handheld scopes have for several years ohmically isolated their inputs from the case and ground, they have not previously offered isolation among the scope channels. Like the scope, the DMM provides four channels. Each is independent of the others and offers true-rms-responding ac measurements with 50-kHz bandwidth and 8000-count, or approximately 13-bit, resolution.

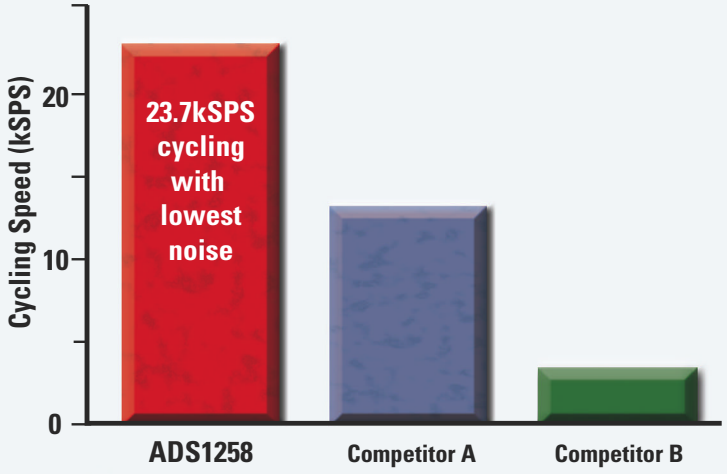
The instrument also provides as standard features an FFT analyzer, a harmonic analyzer, and a data recorder that can take DMM readings as rapidly as every 800 µsec or, at lower sampling rates, can record for as long as a month. Although 12-bit resolution is uncommon in scopes—especially those with 320×240-pixel, 5.7-in. backlit, color touchscreen LCDs—the high ADC resolution compared with that of 8-bit instruments provides 24-dB better FFT and harmonic-analyzer dynamic range for voltage measurements.

**—by Dan Strassberg**

▷**AEMC**, www.aemc.com.
▷**Agilent Technologies**, www.agilent.com.

DILBERT By Scott Adams

# Fastest Cycling 24-Bit ADC




The **ADS1258** 16-channel, 24-bit ADC from Texas Instruments features the lowest latency, fastest channel cycle rate and lowest noise of any competitive devices. With a measurement latency of 42µs, the ADS1258 can measure all of its 16 input channels in less than 675µs with only 12µVrms of input referred noise, offering unmatched performance for precision, multi-channel data acquisition applications.

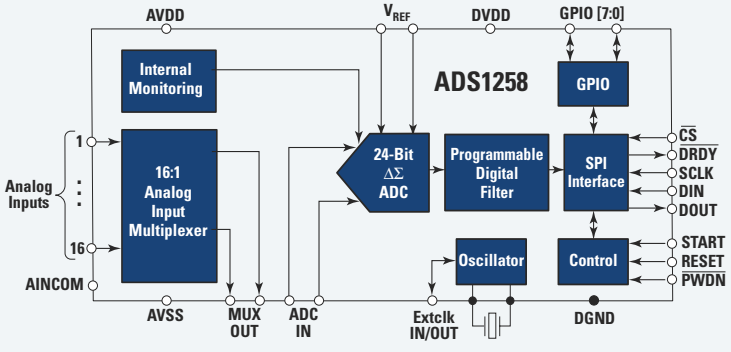
Burr-Brown Products from Texas Instruments

## ▸ Applications

- Industrial process control
- Medical/patient monitoring
- Data acquisition
- Test and measurement
- Instrumentation

## ▸ Features

- 16-channel, 24-bit ADC
- Latency: 42µS
- Cycling data rate: 23.7kSPS
- Measure all 16 inputs in only 675µs
- Programmable digital filter 2.8µVrms noise at 1.8kSPS data rate
- Unipolar (+5V) or bipolar (±2.5V) operation
- INL: 0.0010% (max)
- Offset drift: 0.1µV/°C
- Package: QFN-48
- Pricing: $7.95 in 1k units

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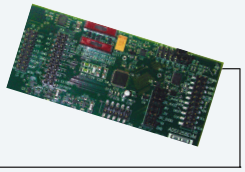

**www.ti.com/ads1258 ○ 800.477.8924, ext. 13497**

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Texas Instruments

# Midrange device includes SERDES function

Lattice Semiconductor has announced a mid-capacity, midpriced FPGA that includes some of the high-speed, high-end functions you typically find only in the most advanced and priciest Xilinx (www.xilinx.com) Virtex and Altera (www.altera.com) Stratix FPGAs. The company's new ECP2M FPGA family adds high-speed embedded SERDES (serializer/deserializer) I/O plus a pre-engineered PCS (physical-coding-sublayer) block to the company's midrange-FPGA lineup.

Shakeel Peera, director of strategic marketing for high-performance-FPGA products at Lattice, says that, over the last few years, the high-end telecommunications and storage markets have been demanding SERDES blocks. FPGA vendors responded by offering these blocks in their high-end FPGAs. "Demand for SERDES has expanded beyond telecom and storage markets," says Peera. "The industrial, automotive, broadband-access, and consumer-electronics markets are also interested in FPGA technology. High performance is now the domain of not only the low-volume, high-end FPGA market, but also the high-volume, medium-density market." However, Xilinx's and Altera's low-cost, high-volume FPGAs, Spartan and Cyclone, respectively, lack SERDES functions. "The big guys haven't put these functions into their midrange devices because they are worried about cannibalizing their high-end devices," says Peera.

Now, with the ECP2M FPGA family, Lattice offers four to 16 channels of 3.125-Gbps SERDES in a quad-based architecture ranging from one quad to four quads, with each quad including four SERDES channels. The device also includes PCS with 8b/10b encoding, an Ethernet-link state machine, and rate-matching circuitry. This SERDES/PCS combination suits the device for PCI Express; Gigabit Ethernet; Serial RapidIO; and wireless-interface standards, such as OBSAI and CPRI. "Because we added the high-speed I/O, we also increased the on-chip RAM by five to six times over the previous parts in the ECP2 family," says Peera.

> "High performance is now the domain of not only the low-volume, high-end FPGA market, but also the high-volume, medium-density market.

The new Lattice ECP2M family includes five devices ranging in density from 20,000 to 95,000 look-up tables. The devices will feature 24 to 168 18×18-bit multipliers, two DLLs (delay-locked loops), and eight PLLs (phase-locked loops) for timing control. Lattice offers the devices in fine-pitch BGA packages with 144 to 601 I/O pins. The devices operate from 1.2V power supplies. Lattice's first product in the family, the ECP2M-35, costs $22.95 (100,000) and will be available in 2007. Stan Kopec, vice president of marketing, claims that the price is roughly one-third that of the competition's products and that the part will address approximately 80% of SERDES applications.

**—by Michael Santarini**

▷**Lattice Semiconductor**, www.latticesemi.com.

# Flexible switch has 48 lanes

Switches are key components of systems based on the emerging PCIe (PCI Express) standard. The more capable the switch, the more design flexibility that developers enjoy. PLX Technology has now introduced one of the most flexible PCIe switches currently available, the PEX 8548. This device offers 48 PCIe lanes that designers can allocate across as many as nine ports in a variety of configurations.

The PEX 8548 targets high-performance graphics and PCIe fan-out applications, but the switch's flexibility makes it suitable for a variety of designs. The device has a nonblocking switch architecture, enabling it to offer peer-to-peer transfers that can operate in parallel with other transfers through the switch. Cut-through latency is less than 110 nsec. The nine ports are configurable, allowing users to allocate the 48 available lanes as one, two, four, eight, or 16 ports. Thus, for graphics applications, the device can offer three 16-lane ports. As a fan-out switch, it can offer six eight-lane ports, four four-lane ports, four eight-lane ports, or many other combinations.

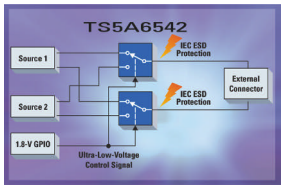

Designers can use the PEX 8548 switch in a variety of configurations. It offers 48 PCI Express lanes that designers can allocate across as many as nine ports.

The device complies with PCIe 1.1, and three of its ports support hot-plug operation. It offers a JTAG interface for test and $I^2C$ for out-of-band control. An EEPROM for power-up configuration is available as an option. The device costs $65 (high volumes), will be available for sampling in the fourth quarter, and should be in full production in early 2007.

**—by Richard A Quinnell**

▷**PLX Technology**, www.plxtech.com.

# Analog Switches from Texas Instruments



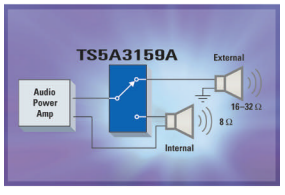

▶ **Single SPDT analog switch with input logic translation and IEC ESD (TS5A6542)**

– +/- 15kV IEC 61000-4-2 Contact Discharge ESD protection (common pin)

– Low ON-state resistance (0.75Ω max)

– Excellent ON-state resistance matching

– Break-before-make switching



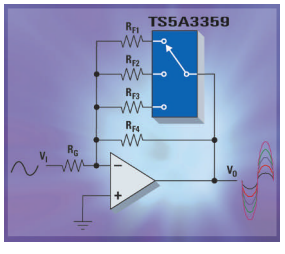

▶ **Single 0.9-Ω SPDT analog switch (TS5A3159A)**

– 100-MHz bandwidth – highest of any 3159-type in the industry

– Ultra-small wafer chip scale packaging

– Wide low-voltage operating range: 1.65 V to 5.5 V

– Break-before-make switching




▶ **Single, 0.9-Ω SP3T analog switch (TS5A3359)**

– Space-saving integration eliminates the need for using serial connected SPDT analog switches

– Isolation in the powered down mode (V+ = 0V)

– 1.65-V to 5.5-V single-supply operation (Control Inputs are 5.5 V tolerant)

– Break-before-make switching

| Device | $r_{on}$* (Ω) (max) | $r_{on}$ Flatness (Ω) (max) | $r_{on}$ Mismatch (Ω) (max) | $V_+$ (V) (min) | $V_+$ (V) (max) | ON Time (ns) (max) | OFF Time (ns) (max) | Pins/Packages |
|---|---|---|---|---|---|---|---|---|
| **SPST** | | | | | | | | |
| TS5A3166 | 0.9 | 0.15 | — | 1.65 | 5.5 | 7 | 11.5 | 5/SC70, SOT-23, WCSP |
| TS5A3167 | 0.9 | 0.15 | — | 1.65 | 5.5 | 7 | 11.5 | 5/SC70, SOT-23, WCSP |
| TS5A4594 | 8 | 1.5 | — | 2.7 | 5.51 | 7 | 14 | 5/SC70, SOT-23 |
| TS5A4595 | 8 | 1.5 | — | 2.7 | 5.51 | 7 | 14 | 5/SC70, SOT-23 |
| TS5A4596 | 8 | 1.5 | — | 2.7 | 5.5 | 17 | 14 | 5/SC70, SOT-23 |
| TS5A4597 | 8 | 1.5 | — | 2.7 | 5.5 | 17 | 14 | 5/SC70, SOT-23 |
| TS5A1066 | 10 | 5 | — | 1.65 | 5.5 | 5.5 | 4.5 | 5/SC70, SOT-23, WCSP |
| **SPST x 2** | | | | | | | | |
| TS5A23166 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 7.5 | 11 | 8/US8, WCSP |
| TS5A23167 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 7.5 | 11 | 8/US8, WCSP |
| **TS3A4741** | 0.9 | 0.4 | 0.05 | 1.65 | 3.6 | 14 | 9 | 8/SSOP, MSOP |
| TS5A2066 | 10 | 5 | 1 | 1.65 | 5.5 | 5.8 | 3.6 | 8/SM8, US8, WCSP |
| **SPST x 4** | | | | | | | | |
| **TS3A4751** | 0.9 | 0.4 | 0.05 | 1.65 | 3.6 | 14 | 9 | 14/TSSOP |
| **SPDT** | | | | | | | | |
| **TS5A6542** | 0.75 | 0.25 | 0.25 | 2.25 | 5.5 | 25 | 20 | 8/WCSP |
| TS5A4624 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 22 | 8 | 6/SC70 |
| TS5A3153 | 0.9 | 0.15 | 0.1 | 1.65 | 5.5 | 16 | 15 | 8/US8, WCSP |
| TS5A3154 | 0.9 | 0.15 | 0.1 | 1.65 | 5.5 | 8 | 12.5 | 8/US8, WCSP |
| TS5A3159A | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 30 | 20 | 6/SC70, SOT-23, WCSP |
| TS5A3159 | 1.1 | 0.15 | 0.1 | 1.65 | 5.5 | 35 | 20 | 6/SC70, SOT-23 |
| TS5A3160 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 6 | 13 | 6/SC70, SOT-23 |
| TS5A3157 | 10 | 5 | 0.2 | 1.65 | 5.5 | 8.5 | 6.5 | 6/SC70, SOT-23, WCSP |
| TS5A63157 | 10 | 2 | 0.14 | 1.65 | 5.5 | 5 | 3.4 | 6/SC70, SOT-23 |
| TS5A2053 | 13.8 | 4.5 | 4.5 | 1.65 | 5.5 | 6.8 | 4.1 | 8/SM8, US8 |
| **SPDT x 2** | | | | | | | | |
| **TS5A23159** | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 13 | 8 | 10/MSOP, QFN |
| TS5A23160 | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 5.5 | 10 | 10/MSOP |
| TS5A23157 | 10 | 4(typ) | 0.15(typ) | 1.65 | 5.5 | 5.7 | 3.8 | 10/MSOP |
| **SPDT x 4** | | | | | | | | |
| TS3A5018 | 10 | 7 | 0.8 | 1.65 | 3.6 | 8 | 6.5 | 16/SOIC, SSOP (QSOP), TSSOP, TVSOP,QFN |
| **SP3T** | | | | | | | | |
| **TS5A3359** | 0.9 | 0.25 | 0.1 | 1.65 | 5.5 | 21 | 10.5 | 8/US8 |
| TS5A3357 | 15 | 6.5(typ) | 0.1(typ) | 1.65 | 5.5 | 6.5 | 3.7 | 8/SM8, US8 |
| **SP4T x 2** | | | | | | | | |
| TS3A5017 | 12 | 9 | 2 | 2.3 | 3.6 | 9.5 | 3.5 | 16/SOIC, SSOP (QSOP), TSSOP, TVSOP, QFN |

**Data measured under typical conditions with maximum $V_+$.*
*Data collected as of 7/06*

*New Products are listed in **bold red.***

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**5-ball/6-ball WCSP (YZP)**
Ball pitch = 0.020 mm (0.50 mm)
Height = 0.020 mm (0.50 mm)
Area = 0.002 mm (1.26 mm)


**10-pin QFN (RSE)**
Lead pitch = 0.020 mm (0.50 mm)
Height = 0.039 mm (0.60 mm)
Area = 0.005 mm (3.18 mm)

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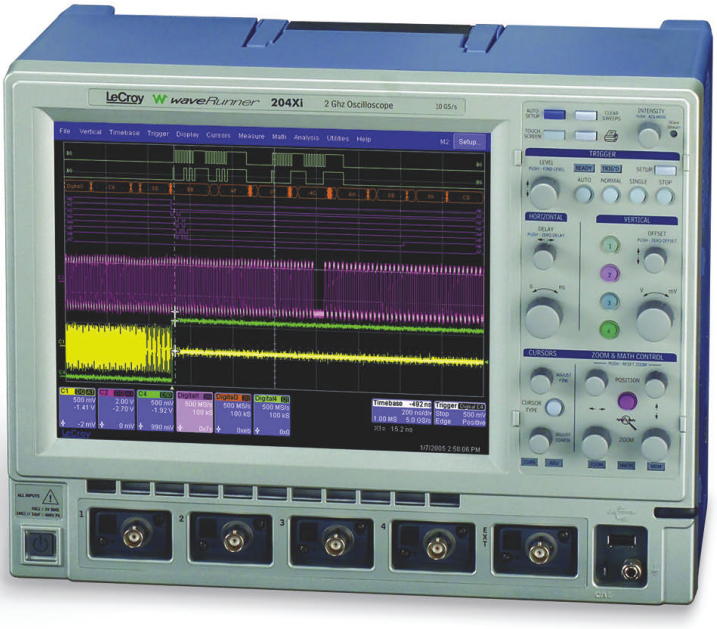
# DSOs find and display anomalous waveforms before you can explain why they are unusual

One of the most frustrating aspects of using a digital scope to diagnose intermittent malfunctions in a UUT (unit under test) is that, to get the scope to display the anomalous waveforms, you generally must describe to it what is unusual about those waveforms. However, until you can see the anomalies, you can't describe them. Is the problem a runt pulse, a slow or misplaced edge, a unit interval of slightly incorrect length? You don't know, and, because a quick glance at a large group of waveforms may reveal nothing unusual, even scopes that let you use normal waveforms to create a trigger mask often fail to provide the needed insights.

Many EEs are likely to characterize the WaveScan feature of LeCroy's WaveSurfer and WaveRunner series of large screen, small-footprint (6-in.-deep) digital oscilloscopes as the ultimate scope-based troubleshooting aid, based on the degree of automation the feature brings to the identification of elusive malfunctions. WaveScan-equipped scopes can determine which anomalies are significant and then find the few that exist among thousands of nearly identical signals. The company has made the feature standard on all members of the two scope families, whose bandwidth, with the addition of new models, now extends to 2 GHz (WaveRunner) and 1 GHz (WaveSurfer).




Despite its small package, the WaveRunner 204Xi 2-GHz-bandwidth digital scope incorporates the WaveScan feature, which can find elusive waveform anomalies without your even having to know what they look like.

## FROM THE VAULT

**"The medical system 25 years from now promises to fulfill the hopes of both science-fiction writers and doctors: It will be efficient and life-saving. And computer technology will hold the key."**

Susan Rabinovitz, *EDN* staff assistant, *EDN*, Oct 14, 1981, pg 293.

WaveScan finds aberrant waveforms without your having to tell it—or even know—what unusual signal characteristics to look for. It then displays only the atypical signals. Moreover, it can do so either in real time—as waveforms arrive—or retrospectively on previously captured signals. Hence, in a UUT that fails intermittently, WaveScan can unearth the associated anomalous waveforms and provide statistical analyses of their salient parameters without your having to figure out what conditions to use as criteria.

The tool accomplishes this feat by measuring multiple parameters of each waveform, finding the norm for each characteristic, and determining—based on your estimate of how far out on the tails of the probability distribution the interesting waveforms lie—whether each waveform's measured values constitute an abnormal set. However, if you want to tell WaveScan what anomalous characteristics to look for, the tool lets you specify them in exquisite detail. As Director of Product Management Mike Lauterbach, PhD, points out, scope users have been clamoring for such a capability for years.

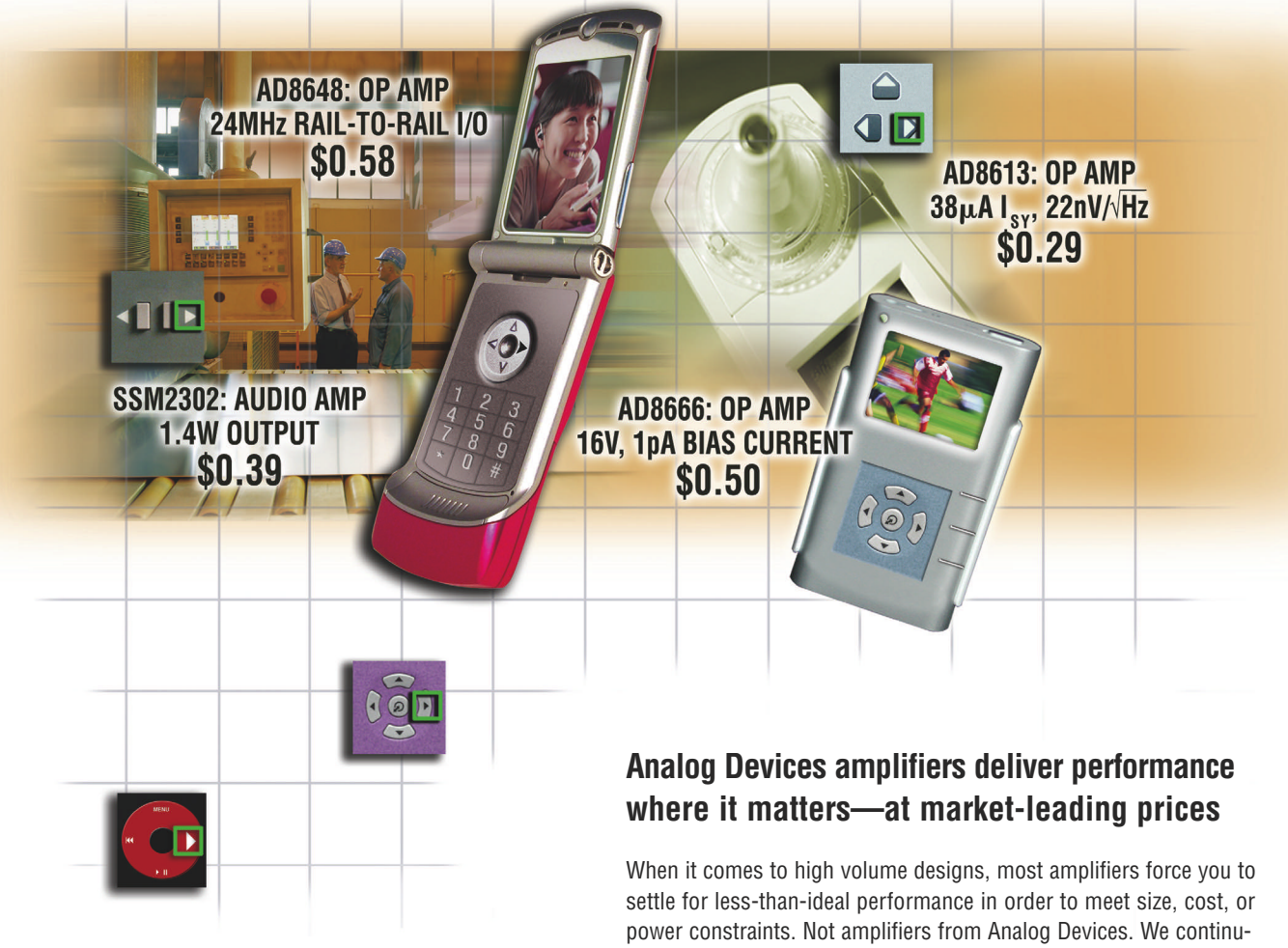
In the WaveRunner line, the new models are the $22,250, 2-GHz-bandwidth 204Xi and the $16,250, 1-GHz 104Xi. Both acquire 5G samples/sec on four channels simultaneously and 10G samples/sec on two channels. In the WaveSurfer line, the new model is the $12,890, 1-GHz 104Xs. This unit acquires 2.5G samples/sec on four channels simultaneously and 5G samples/sec on two channels.

LeCroy has also announced a new series of small, low-cost, high-impedance scope probes with bandwidths of 1.5 GHz and 900 MHz for $1190 and $490, respectively. Input impedance is 1 MΩ in parallel with 0.9 pF. The 1.5-GHz probes allow the use of 1-GHz-bandwidth scopes at full bandwidth; the 900-MHz units allow use of 600-MHz scopes at full bandwidth. The ZS probe family includes a large group of tips and ground-lead accessories for accessing hard-to-reach signals with minimum degradation at high frequencies.

**—by Dan Strassberg**

▷**LeCroy Corp**, www.lecroy.com.

# Amplifier pricing where you want it, performance where you need it, analog is everywhere.




## Analog Devices amplifiers deliver performance where it matters—at market-leading prices

When it comes to high volume designs, most amplifiers force you to settle for less-than-ideal performance in order to meet size, cost, or power constraints. Not amplifiers from Analog Devices. We continuously innovate to give designers the best combination of performance, functionality, price, power consumption, and support.

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ANALOG DEVICES

# IC tool ensures proper heat dissipation

IC-power-analysis-tool vendor Apache Design Solutions has introduced a static-thermal-analysis tool for locating potential heat problems in ICs. Until now, only one other company—Gradient Design Automation (www.gradient-da.com)—offered on-chip thermal-analysis software. According to Apache's president and chief executive officer, Andrew Yang, the new Sahara-PTE (power-thermal-electrical) tool, ties closely to Apache's RedHawk power-analysis and PsiWinder electrical-analysis tools because thermal analysis directly relates to power and affects timing. Timing, in turn, impacts power, which affects thermal integrity.

Yang says that, starting at the 65-nm node, designers must monitor heat generation by monitoring switching and leakage power, and they must analyze parts of the IC and the package to ensure that heat dissipates properly from paths through the substrate, to the package, the heat sink, and even the metal layers. The priority, however, is to ensure that heat and leakage don't escalate into a thermal runaway. "At 65 nm, thermal-analysis tools are nice to have, but, at 45 nm, they become mandatory," says Yang, who notes that the first thermal-integrity tools are static, but future thermal tools will need to become dynamic to more accurately analyze thermal integrity in multiple modes and in multiple ambient conditions.

To analyze thermal integrity, Apache outlines two flows for Sahara. In the PT (power-thermal) loop, users analyze temperature and power across the chip for a given period of clock cycles. This analysis runs with Apache's RedHawk and Sahara-PTE. It provides users with a condition in which the design achieves equilibrium over several clock cycles for both power and temperature. During the analysis, if heat and leakage continue to rise for each iteration and clock cycle, the design may be reaching thermal runaway, so users must shift around some functions or find a way to dissipate heat or cool the device.

The PsiWinder flow electrically analyzes the PT loop, creating the PTE loop. In this flow, users analyze the temperature-dependent resistances of the devices. The PTE flow helps to monitor changes in current density and interconnect self-heating, both of which can impact voltage drop, timing, and power and can contribute to or cause electromigration. Both the PT and PTE flows require Apache's library-characterization technology.

PTE-flow inputs include a cell library, LEF (library-exchange format), DEF (data-exchange format), GDSII (Graphic Design System II), an electrical-package model, and a thermal model of the package. If the package is custom or is yet undetermined, users can provide Sahara with a boundary temperature. You can use Sahara-PTE as a stand-alone device with third-party-supplied power and electrical tools, but it works better when running all Apache tools, according to Yang. A one-year subscription for Sahara-PTE has a list price of $160,000.

**—by Michael Santarini**

▷**Apache Design Automation**, www.apache-da.com.

## FEEDBACK LOOP

**"Perhaps you haven't heard about BEST (boasting engineering, science, and technology). ... Approximately 650 high-school and middle-school teams will compete, involving about 6500 students in the engineering process."**

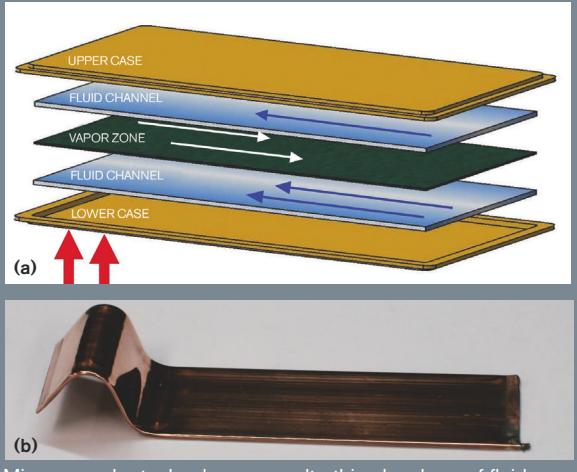
Michael Blazer, in *EDN*'s Feedback Loop at www.edn.com/article/CA6363908. Add your comments.

## ULTRATHIN HEAT SPREADER USES FLUID CORE TO COOL PROCESSORS, DISPLAYS

10.26.06

**Power-hungry components, such as graphics processors and LED displays, currently use a combination of heat spreaders, pipes, and fans to dissipate heat. However, fans introduce reliability concerns, and pipes are bulky. The Microspreader, a new heat spreader from Celsia, uses ultrathin chambers of fluid divided by a 1.44-mm-thick vaporization zone and boasts a thermal conductivity of more than 5000W/mK, compared with 386W/mK for copper or 205W/mK for aluminum—two common heat-spreader materials. As an example of the price performance of the Microspreader, George Meyers, Celsia's vice president of sales, claims that a similarly priced, smaller, lighter, and more reliable Microspreader could replace a $4 fan assembly in a PC.—by Margery Conner**

▶**Celsia Technologies,** www.celsiatechnologies.com.




Microspreader technology uses ultrathin chambers of fluid divided by a vaporization zone (a) to create a heat spreader with much higher thermal conductivity than conventional spreaders based on copper or aluminum (b).

LEADING inside

A series of engineering insights
by Analog Devices.

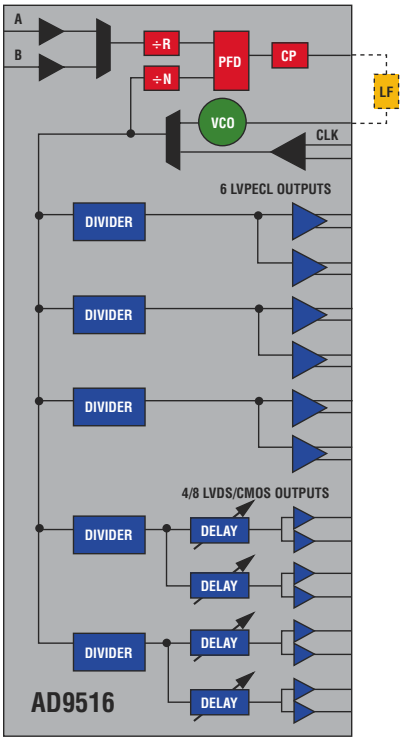
# Single-Chip Clock Generator with 14-Channel Distribution Solves Timing Challenges in Networks

Global demand for communication services continues to rise, and manufacturers must constantly reduce the size and cost of newly installed network equipment, while holding to high standards of service and quality. Part of building a robust network is managing clocks. Clock and timing requirements range from system-level synchronization of wired and wireless network hubs, to local signal distribution inside high density transceiver cabinets. To meet this wide array of design challenges, companies employ signal integrity experts to interpret specifications, oversee testing, and recommend components guaranteed to maintain clean, low jitter clocks throughout the network.

Ask any signal integrity expert about time jitter, and he/she is likely to outline the challenges posed by distributed components, which one-by-one, eat into the system's total jitter budget. Time jitter on clocks is a measure of edge uncertainty. All systems can tolerate some amount of clock edge uncertainty. But when clock edges occur at increasingly random times, the system begins to break down. Missing one clock cycle may result in transmitters and receivers getting out of sync.

When time jitter limits a system's overall signal-to-noise ratio or bit error rate, data may be lost. In a mobile network, this can lead to reduced call quality, or even dropped calls.

Consider a system that requires four clock functions in series: frequency multiplication, frequency division, phase offset, and level translation. If each function is performed by a separate component, the time jitter of each device must be mathematically combined to calculate the total clock path jitter. Four cascaded components, each with a jitter specification of 1.5 picoseconds (ps) rms, yield a total jitter of 3 ps rms (note: the square root of the sum of squares approach applies). Therefore, the complete clock path has twice the jitter of individual components.



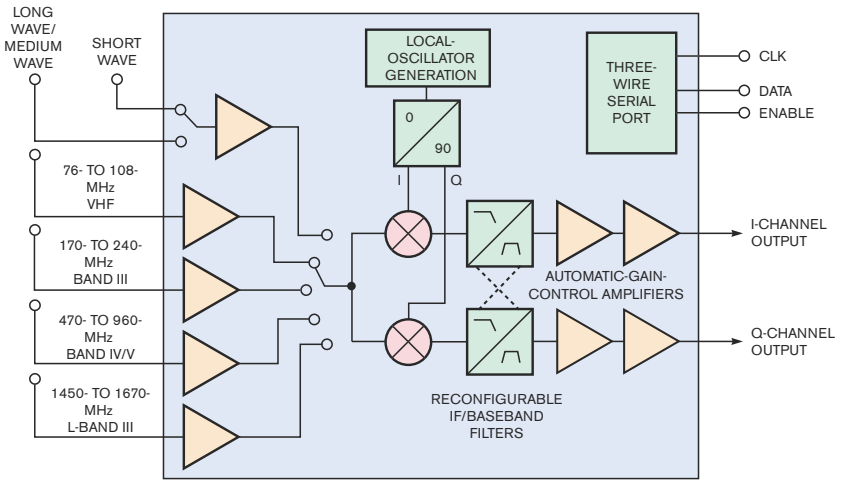

*Integrated timing functions in a single 9 mm × 9 mm, 64-lead LFCSP control jitter to below 1 ps rms*

Now compare this to a solution where all critical timing functions are integrated into a single device—a complete phase-locked loop (PLL), including the voltage controlled oscillator (VCO) for frequency multiplication, five channel dividers with built-in phase offset capability, and clock output drivers offering the choice of LVPECL, LVDS, or CMOS levels. With the integrated approach, total clock path jitter may be controlled to well below 1 ps rms.

Analog Devices' AD9516, integrated 2.8 GHz clock generator with 14-channel distribution, enables network designers to generate 14 clean, low jitter clocks from a single chip. In addition, the AD9516 offers low time skew between its six LVPECL outputs. This capability means that designers are assured that all six clock edges occur within a well-defined time window. The LVDS/CMOS channels include programmable delay lines which may be used to compensate for delays in other parts of the system. Two inputs—A and B—feature automatic switchover, providing protection in the event of reference clock failure. Finally, because standalone oscillators are one of the most likely components to fail in a network, the AD9516 improves overall system reliability by integrating the VCO on-chip.

Analog Devices offers a wide range of clock and timing solutions that enable signal integrity engineers to maintain performance while reducing the size and cost of new equipment. For data sheets, free samples, and more information, visit *www.analog.com/clock-timing-AD9516.*

*Author Profile: **Scott Behrhorst** is marketing and applications manager for Analog Devices' Clock and Signal Synthesis product line.*




The MS1001 RF-tuner IC covers multiple broadcast standards at 100 kHz to 1.9 GHz.

GLOBAL DESIGNER

# Single-chip receiver for mobiles handles TV and radio

Start-up Mirics Semiconductor describes its new MS1001 RF-tuner IC as a "polyband" device for mobile digital-broadcast reception. Although several companies have recently made announcements that focus on the mobile-TV sector, Mirics says that its chip has much wider applicability, covering multiple broadcast standards. The chip covers broadcast bands ranging from 100 kHz to 1.9 GHz.

The primary target market is the mobile phone. The company forecasts that, by 2009, some 20% of all phones will have mobile TV, but a much higher proportion will have radio capability, and the fraction that does have TV will encompass numerous standards. Mirics aims to provide the receiver function for TV and radio at the same cost and power level as FM radio alone. All the chip's signal processing is analog, and the chip reconfigures and reconnects its on-chip functional blocks in response to external commands, depending on the band and signal type. This reconfiguration extends to the basic architecture of the receiver function. In some cases, the receiver uses a direct-conversion, zero-IF layout; in others, it uses a conventional heterodyne architecture. The MS1001 has five RF inputs with individual on-chip low-noise amplifiers. It yields quadrature output signals, and you use a three-wire serial digital port to control the device's configuration, which you can change dynamically. As well as providing a single receiver chip for all bands, Mirics asserts that its product is the cheapest and lowest power device available, at $3.50 (10,000). Mirics aims to further reduce the cost to make the device competitive with chips that provide the FM function alone and to exploit mixed-signal capability to add a flexible on-chip digital demodulation capability.

**—by Graham Prophet**
***EDN Europe***

▷**Mirics Semiconductor**, www.mirics.com.

10.26.06

## ENTERPRISE NETWORKS TOUT 10-GBPS SPEED

**Systimax Solutions is building upon its proprietary network-analysis tools and techniques to create reliable and high-performance structured cabling. The company recently introduced the 10-Gbps GigaSpeed X10D UTP (unshielded-twisted-pair) copper cabling. The cabling has met the Cisco (www.cisco.com) Technology Developer Program criteria for interoperability with Cisco Unified Communication products. Using proprietary modal-decomposition-modeling, connector-field-pattern modeling, and cable-twist-accuracy technologies, GigaSpeed X10D minimizes alien crosstalk–an impairment to 10-Gbps Ethernet's adoption. Alien crosstalk is the undesired coupling noise between adjacent cables and connectors. Failure to minimize this crosstalk results in inferior transmission performance and insufficient bandwidth to ensure reliable 10-Gbps performance.**

**"For a 10-Gbps UTP to both comply with industry standards and operate in today's sophisticated enterprise networks, it must satisfactorily address the issue of alien crosstalk," says David Haley, industry consultant for market researcher Acuity (www.acuity-mi.com). "If you don't eliminate a significant amount of this crosstalk within the design of the cabling channel, you don't have a 10-Gbps technology. Because of its strong engineering and testing, Systimax Solutions' technology addresses the current and future needs of the enterprise network, which is a key characteristic of companies involved in the Cisco Technology Developer Program."**

**"Cisco supports open, standards-based architectures and shares a commitment to interoperable systems with Systimax Solutions," says Cherie Reed, manager of the Cisco Technology Developer Program. "Through this vision, the program delivers the power of choice to enterprises or service providers–the ability to extend the Cisco end-to-end architecture with our participants' solid products and technologies."**

**—by Vinod Kataria, *EDN Asia***

▶**Systimax Solutions,** www.systimax.com.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Agilent Technologies

# VOICES

## HP's Paul Tuttle: the man in the moon

After a stint in the Air Force, Paul Tuttle started his career in 1966 with Filtron, which provided RFI testing on everything from Caterpillar tractors to NASA space hardware. That's how his name ended up on the moon, engraved on pieces of Surveyor 3. After leaving Filtron, he worked at RCA as a technician. When the recession of the 1970s hit, engineers were taking jobs as technicians, so he went to college to further his education under the GI bill. Before he could get his degree, a tiny company called AutoWeigh hired him. He then moved to Smith Kline Medical Systems and, later, Ekoline Instruments, which led to his long career at Hewlett-Packard.

**When did you go to work for HP?**

A I guess 1973 is when I officially started with Hewlett-Packard. Interesting that I applied for a job at Hewlett-Packard in 1972 or 1973 but didn't get the job, so later HP had to buy my company to get me aboard.

**You were there 28 years. I understand your father was an early employee?**

A Yes, he was one of the first 700 employees of Hewlett-Packard, a pioneer of sorts; he started in 1948 and retired after 35 years. We overlapped by a year or so.

**Is your father's involvement in HP what brought you to the company?**

A In a way, I guess. I used to go to the company picnics at Adobe Creek Lodge when Dave [Packard] and Bill [Hewlett] cooked the hamburgers. I think I always knew that Hewlett-Packard was a good company; I just didn't know it was a great company until much later.

**Toward the end of your career, you were at the HP automotive-systems division. What happened then?**

A The automotive-division management team made some strategic decisions that didn't work out well; business in the automotive group dropped dramatically, and, like any other business, it closed. I took a new position at a recent acquisition, VeriFone, and moved on. A couple of years later and with new Hewlett-Packard leadership, management deemed VeriFone as a nonstrategic move and spun it off. Having met the criteria for retirement—55 and with more than 15 years of service—I decided to stay with VeriFone and instantly retired from HP. I stayed with VeriFone for another year before our engineering team was dissolved, and I finally got the message and retired.

**Did you know any of the HP executives?**

A Yes, and they were professional, friendly, and approachable. The "HP Way" was still in effect then.

**Was the HP Way real?**

A Absolutely, and the company adhered to it almost religiously. Basically, the HP Way was nothing more than having respect for fellow employees and being a good corporate citizen.

**Was Carly [Fiorina] good for HP?**

A No, she was and is a marketer—not something Hewlett-Packard needed in such a high-management position.

**Would you have split off Agilent?**

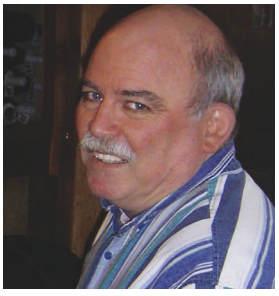
A No, the core business of Hewlett-Packard was test equipment. That's now Agilent's business. The complementary services between the two companies could only make a bigger Hewlett-Packard stronger. I also didn't like Agilent's selling off the medical arm of the company, which Hewlett and Packard themselves considered a crown jewel of the old Hewlett-Packard.

**Would you have bought Compaq?**

A No, and I actively fought against it.

**What do you think the future holds for HP and Agilent?**

A Hewlett-Packard is in good hands now. Mark Hurd is the right man for the chief-executive-officer job. The results are already showing in the bottom line of the quarterly reports. Plus, the employees are more at ease,



and productivity is up. Agilent is still an open question. With the recent consolidation of headquarters and the Agilent Labs into the Santa Clara site and the paring off of marginal operations, Agilent is getting tighter and tougher. Perhaps that's a good thing. I still own stock in both of them.

**Is the HP Way dead?**

A It pretty much was under Fiorina's leadership, but Hurd has seemingly brought it back to life. He has problems with MBWA [management by walking around], but he is a very nice, approachable young man with a self-deprecating sense of humor. That filters down to lower levels of management and that comfortable feeling nourishes others. When you're comfortable in your job, you show more respect for fellow employees; that's a basic function of the HP Way.

**HP used to always top the list as a great place to work. What's happened?**

A I believe Hewlett-Packard will soon return to the listings of a great place to work. A major portion of the requirements of what constitutes a great place to work comes from financial results. HP has recently been poor in that area, but things are getting better, and so will Hewlett-Packard.

**—Paul Rako**

R A Q ' s

# Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

## The Long Term Stability of Precision Analog ICs, or How to Age Gracefully and Avoid Sudden Death

**Q.** *The life expectancy of my product is 20 years. How well will its calibration survive?*

**A.** Quite well, actually. Provided you protect it from abuse.

I am, alas, too fond of good one-liners. When asked how precision analog ICs age I usually answer "gracefully" or "365 days per year". But although these answers *are* true they are not always very helpful.


Precision analog ICs are very stable devices. Unlike wine they do not actually improve with age, but typically they have long-term age-related changes of around 1 ppm/thousand hours (the value may be given on the data sheet). It is important to realize that this aging is not cumulative, it obeys a "drunkard's walk" law. If you want the mathematics of a drunkard's walk you should consult this reference[1], but essentially each consecutive step is in a random direction. For a one-dimensional drunkard's walk this means that the distance from the origin is approximately proportionate to the square root of the number of steps.

So if a device ages at 1 ppm/1000 hours it ages at $\sqrt{2}$ ppm/2000 hours, etc. Since there are 8766 hours in a year (on average, 8760 in a normal year and 8784 in a leap year) 1 ppm/1000 hours = 2.96 ppm/year = 9.36 ppm/decade and 13.24 ppm/2 decades.

This does not vary much between devices that are continually powered, in storage, or have a reasonable range of ambient temperatures. Since this is a statistical process the variation between devices will be as large as the effect itself. High temperatures do accelerate the process, but not by very much, and the characteristics vary with different processes. Unless your circuit is spending the majority of its time above 100°C it is not unreasonable to expect aging to be close to the data sheet rate.

However there is another mechanism that causes ungraceful and abrupt changes of accuracy, and may also increase the rate of subsequent aging. That is electrostatic damage (ESD). It is a popular superstition that ESD is sudden death to an IC and that is often true. A discharge can do a small amount of damage which does not destroy the device, but does affect its performance (and may lead to sudden death later on). Such damage is often one-off but it can be cumulative—we once had a Finnish customer who complained that one of our op-amps got noisier with the passing years. Closer investigation revealed that actually nothing much had happened during the passing Summers, but it had indeed got noisier around the turn of each year, when the cold dry air of a Finnish Winter encouraged much more static electricity.

Adequate ESD protection is essential if an IC is to age gracefully.

[1] http://en.wikipedia.org/wiki/Random_walk

**To learn more about precision analog ICs, Go to: http://rbi.ims.ca/4938-101**

**Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.**

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BY BONNIE BAKER

# Get more accuracy from your DAC

With a DAC, you calibrate by initially determining the code-to-voltage error at one-third of the output range and again at two-thirds of the output range. The range between one-third full-scale and two-thirds full-scale avoids the output amplifier errors near the power-supply rails. The calibration of the offset and gain-error correction is a matter of simple algebra, where $V_{OUT}=a+bV_{IN}$. In this formula, a is the offset error, and b is the gain error. You can accomplish these calibrations in the digital domain with the help of an ADC that is more accurate than a DAC's target specifications. This calibration technique is effective with offset and gain errors greater than 2 LSBs (least significant bits); however, the converter's quantization errors limit this approach.

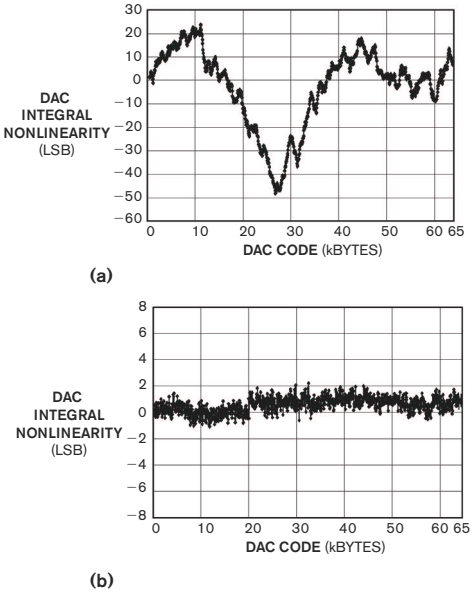



Figure 1 The INL (integral nonlinearity) of a 16-bit string DAC can vary across 10s of codes (a). A correction step of 64 LSB (1024 of the 65,536 points) reduces the INL error to less than ±3 LSB (b).

A more challenging DAC-calibration activity is to adjust the linearity of the converter's entire output range. Once again, you need an ADC that has four times the resolution of the DAC. The temptation is to calibrate every code of the DAC. This strategy may be acceptable for converters with 8, 10, 12, or 14 bits of resolution. This environment has fewer DAC codes to calibrate, the memory requirements are lower, and the accuracy of the calibrating ADC is not as demanding, allowing faster analog-to-digital conversion. For DACs with resolution of more than 14 bits, the total number of codes becomes unmanageable for processors or processor memory. Additionally, you need to use a slower ADC with higher accuracy, such as a delta-sigma converter. Higher cost and lower speeds encourage you to decide that linearizing every code for higher bit DACs is not worth the bother.

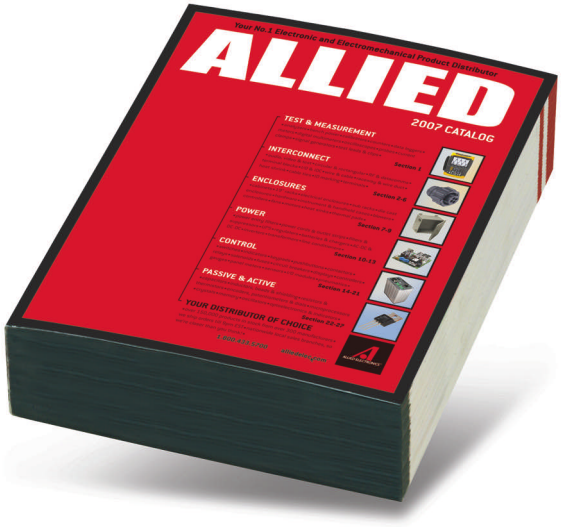
An effective alternative to linearizing every DAC code is to select several small groups of codes. The plot in **Figure 1a** shows an example of the INL (integral nonlinearity) of a 16-bit string DAC. The 16-bit string DAC comprises a string of $2^{16}$ resistors. The universal formula for calculating any DAC-correction code is $DAC_{COR}=INL_V+(INL_V-INL_W)(v-x)/(v-w)$, where $INL_V$ and $INL_W$ are the INL errors of the v and w code, and x is a code between codes v and w. If (v−w) is equal to an integer that is a power of two, you can implement the division with right shifts, reducing the processor-calculation time and complexity. The plot in **Figure 1b** illustrates the benefit of this linearization technique using 1024 code groupings with 64 codes per group.

This technique best suits DACs that are monotonic and that have INL error of more than ±8 LSB. Additionally, you must exercise care when selecting the size of the code sets. If large, sudden jumps occur from one code to the next, as may be the case with R2R architectures, this technique may prove to be counterproductive rather than an improvement of DAC performance. The string-DAC topology best suits this calibration technique because it is inherently monotonic (a requirement for this technique), and jumps from one code to the next are relatively small compared with those of other DAC topologies. EDN

## REFERENCE

Anderson, Russell, and Michael Gurevich, "MSC1211/12 DAC INL Improvement," Application Report SBAA112, Texas Instruments Inc, March 2004, focus.ti.com/lit/an/sbaa112/sbaa112.pdf.

*Bonnie Baker is a senior applications engineer at Texas Instruments and author of* A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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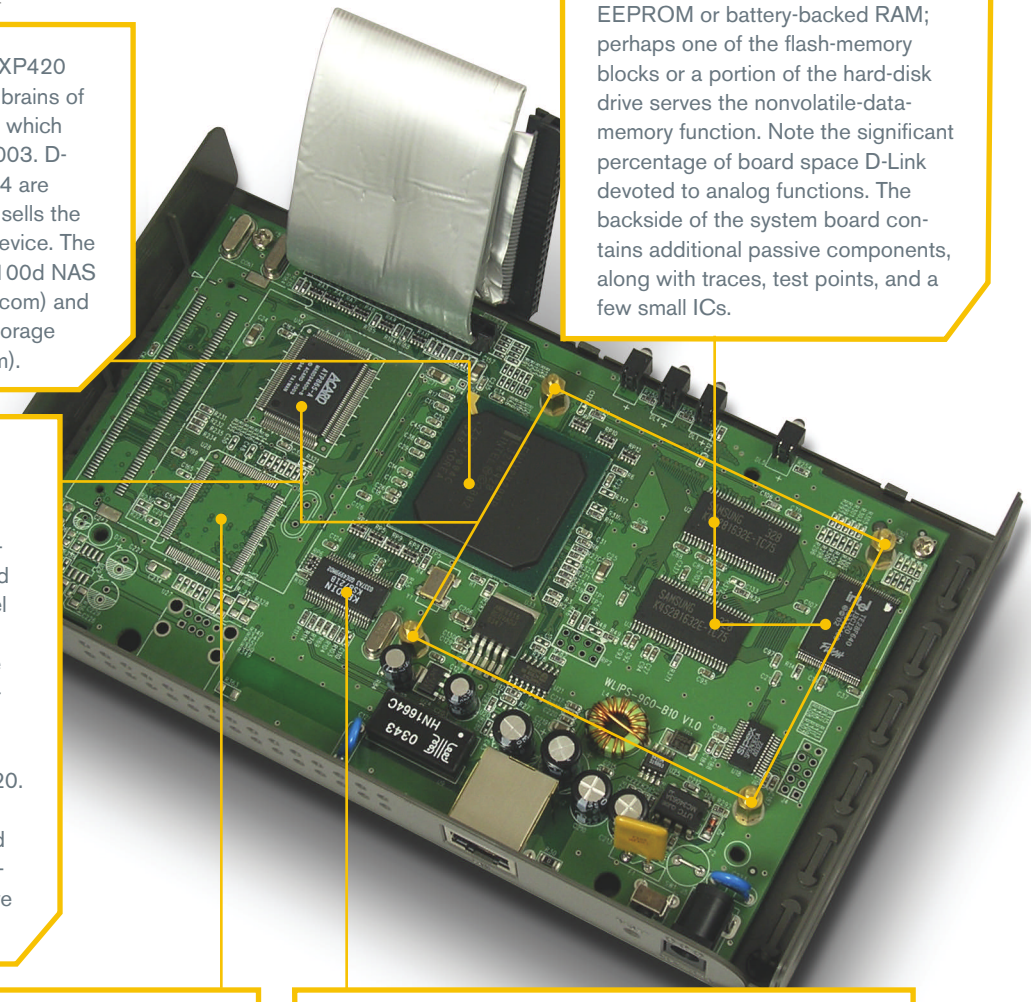
# Mini-NAS: an unfinished masterpiece?

D-Link's (www.dlink.com) DSM-604H Central Home Drive was, as its name implied, one of the first NAS (network-attached-storage) devices that targeted home and SOHO (small-office/home-office) users. Its compact chassis befitted D-Link's stated long-term ambition to append the NAS function to a router. What's under the DSM-604H's hood, and what clues to D-Link's possible future plans does it reveal?

A 266-MHz Intel (www.intel.com) iXP420 network processor constitutes the brains of the now-discontinued DSM-604H, which D-Link introduced in September 2003. D-Link's follow-on DSM-622 and -624 are also obsolete, although D-Link still sells the iXP420-based DSM-G600 NAS device. The iXP420 has also found use in the 100d NAS device from Iomega (www.iomega.com) and in the hacker-embraced NSLU2 Storage Link from Linksys (www.linksys.com).

A 64-Mbit, 120-nsec, 3.3V Intel 28F640 StrataFlash memory and two 3.3V, 128-Mbit, 133-MHz Samsung (www.samsung.com) SDRAMs constitute the semiconductor-memory subsystem. There's no EEPROM or battery-backed RAM; perhaps one of the flash-memory blocks or a portion of the hard-disk drive serves the nonvolatile-data-memory function. Note the significant percentage of board space D-Link devoted to analog functions. The backside of the system board contains additional passive components, along with traces, test points, and a few small ICs.



The other important NAS-device-memory feature is its magnetic rotating storage. The Central Home Drive family came in 20- and 40-Gbyte variants, which the company implemented using 2.5-in., 4200-rpm PATA (Parallel Advanced Technology Attachment) hard-disk drives (whose standoffs are visible in the picture), thereby explaining the unit's svelteness. An Acard ATP865-A PCI-to-IDE controller connects the hard-disk drive to the iXP420. Because the ATP865-A handles two PATA channels, each with primary and secondary drive slots, D-Link conceivably could have developed a multidrive Central Home Drive variant.

Note the prominent, unpopulated IC footprint next to the IDE controller, along with the numerous test points scattered across both sides of the board. Did D-Link have plans for this hardware design, beyond the initial DSM-604H implementation? Was this board an initial-production prototype that the company planned to reduce the cost of in the future? Did D-Link take directly to production an Intel reference design? Or is there another explanation for the hardware exorbitance?

The Central Home Drive has sparse ornamentation; four front-panel LEDs alert the user to active power and device status, along with the presence of active LAN and hard-drive traffic. The back panel encompasses a 5V, 2.5A power plug; a 10/100-Mbit wired-Ethernet connector; and a reset button. Micrel Semiconductor's (www.micrel.com) Kendin KS8721B PHY (physical-layer) chip implements the Ethernet interface with the MAC (media-access-control) transceiver built into the iXP420.

TEXAS INSTRUMENTS

DATA CONVERTERS

Analog Applications Journal

BRIEF

# Using the ADS8361 with the MSP430 USI port

*By Tom Hendrick • Applications Engineer, Data Acquisition Products*

## Introduction

The ADS8361 is a dual, 16-bit, 500-kSPS, analog-to-digital converter (ADC) with four fully differential input channels grouped into two pairs for high-speed, simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differentially to the input of the ADC. This provides excellent common-mode rejection of 80 dB at 50 kHz, which is important in high-noise environments.

MSP430 devices such as the new MSP430F2013, which contain a universal serial interface (USI), can be used in a very simple and straightforward interface that requires no glue logic and very little software overhead. There is no need to shift or concatenate conversion results as was the case in the simple 8-bit SPI interface of the older UART port found in previous generations of the MSP430.

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## Hardware

### ADS8361 EVM

The ADS8361 Evaluation Module (EVM) provides a platform to demonstrate the functionality of the ADS8361 ADC with various TI DSPs and microcontrollers while allowing easy access to all analog and digital signals for customized end-user applications. (For more information on the EVM, see Reference 1.)

### eZ430-F2013 Development Tool

The eZ430-F2013 is a complete MSP430 development tool including all the hardware and software necessary to evaluate the MSP430F2013. The hardware is provided in a convenient USB stick form factor. The eZ430-F2013 uses the Kickstart version of IAR Embedded Workbench integrated development environment (IDE) to provide full emulation with the option of designing a standalone system or detaching the removable target board to integrate into an existing design. This software is available for download at www.ti.com/ez430 under TOOL SUPPORT. The code used in these examples is available upon request.

### Hardware interface

A simple three-wire interface is the minimum requirement to connect the eZ430-F2013 and the ADS8361EVM as shown in Figure 1. The chip select (CS) pin is grounded because only one ADC is placed on the port. If more than one device is on the bus, then chip select should be controlled by any available GPIO on the MSP430 device.

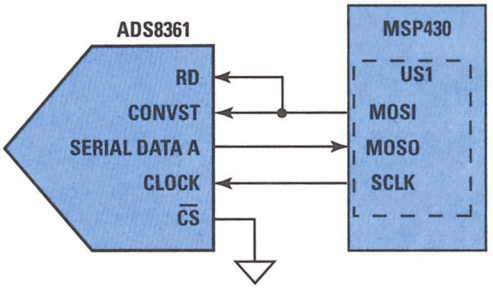


Figure 1. Hardware interface block diagram

## Interface considerations

### MSP430 USI settings

The USI module provides built-in hardware functionality to support synchronous serial communication schemes.

USI control registers 0 and 1 (USICTL0 and USICTL1) set up the basic operation of the serial interface. The port is configured in SPI master mode by setting bits 3, 5, 6, and 7 in USICTL0. The USI counter interrupt is set in USICTL1 to provide an efficient means of SPI communication with minimal software overhead.

The serial clock polarity, source, and speed are controlled by settings in the USI clock control register (USICKCTL). For the purposes of this article, the polarity of the clock is set to zero (dwells low), and the clock source is the SMCLK with a division factor of one.

Bit clocking and shift register configuration are controlled in the USI port by the bit settings in the USI bit count register

(USICNT). The USICNT register has 5 bits that provide up to 32 SCLK cycles per transfer. Setting the USICNT to 0↔13 transmits 19 serial clocks from the MSP430 to the ADS8361 on each conversion cycle. Setting the USI16B bit in the USICNT register causes the shift register to act as a 16-bit transmit/receive buffer. Transmitted data is MSB-aligned and commences with the first SCLK cycle.

### Starting a conversion

With the MOSI output of the USI port connected to both the RD and the CONVST inputs, the ADS8361 will begin to output the conversion results (MSB first) on the fourth SCLK cycle. Since the shift register holds the last 16 bits of received data, the entire 16-bit conversion result is captured for further processing. The timing diagram in Figure 2 shows the entire process.

### ADS8361 operating modes

The ADS8361 has four operational modes controlled by the M0 and M1 pins. The ADS8361EVM provides jumpers to statically set the operating mode. Using GPIO output on the MSP430 permits the operating mode to be controlled by the microprocessor as well.

#### *Two-channel simultaneous sampling*

Selecting ADS8361 Mode I sends serial data on both output channels A and B corresponding to A and B inputs. In Modes I and II, the A0 control input determines if data is sampled from the A0/B0 or A1/B1 input channels. When the A0 control pin is low, the A0/B0 input pairs are sampled and when the A0 control pin is high, the A1/B1 input pairs are sampled. The ADS8361EVM provides a jumper to statically set the input pair via the A0 pin.

Since the eZ430-F2013 has only a single serial port, the ADS8361 must be set to Mode II to send A0/B0 or A1/B1 conversion results through only the Serial Data A output pins (see Figure 3).

#### *ADS8361 channel ID bits*

The serial output stream of the ADS8361 for all modes except Mode I includes channel ID bits so the controller can use software methods to decipher the received channel information. In Mode II, a single A/B ID bit is included in the output data stream. In Mode III, a single 1/0 ID bit is included in both output data streams. Mode IV used both A/B and 0/1 ID bits since all four input conversions are output on one data line.

#### *Four-channel sampling*

Modes III and IV allow the user to realize four-channel operation of the ADS8361 without using the A0 control pin. Mode III provides data from the Serial Data A and B outputs. Mode IV sequentially sends all four conversion results with ID bits via the Serial Data A output. What becomes problematic in this mode when used with the eZ430-F2013 is that the ID bits are essentially lost in the shift register. It is possible to recover these bits via software, but this increases software overhead and adds unnecessary complexity.

When operating in four-channel sequential mode, the ADS8361 can be initialized in such a way that channel integrity can be maintained without the need to decipher the ID bits at all. This requires a simple software loop at the start of the program that sets A0, M0, and M1 to zero. A single conversion is performed to ensure that the ADC is converting inputs A0 and B0. M0 and M1 can then be brought high, which starts sequential conversion of the input channels, starting with A0, B0, A1, and finally B1.

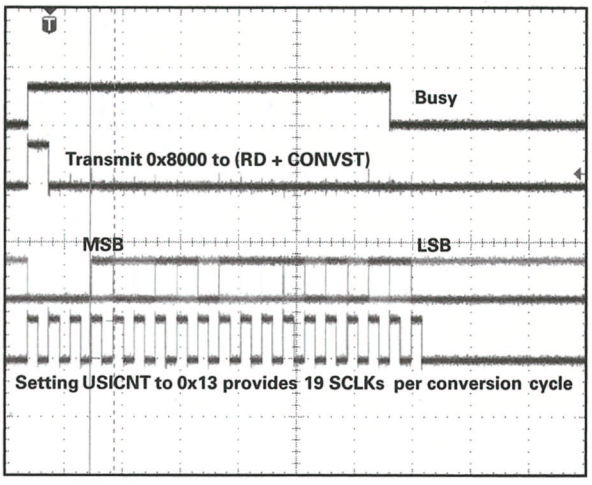


Figure 2. Complete single-channel conversion cycle

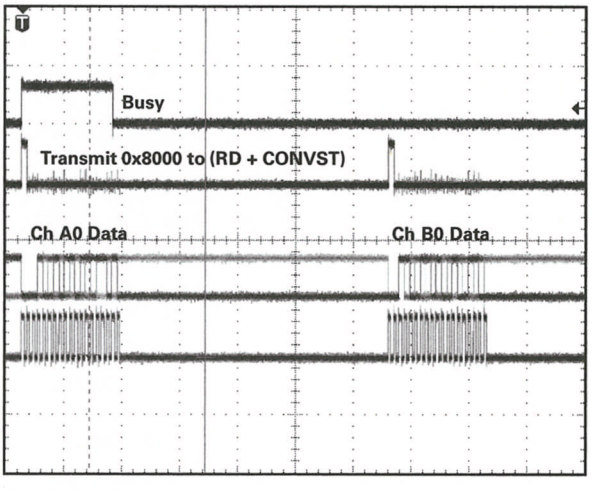


Figure 3. Complete two-channel conversion cycle

## Conclusion

Using the high-performance ADS8361 with the USI port of MSP430 processors brings a new level of flexibility to MSP430 applications that require multichannel, simultaneous data acquisition.


**References:**

1. ADS7861/8361 EVM User's Guide (slau094)
2. ADS8361 Datasheet (sbas230)
3. MSP430x2xx Family User's Guide (slau144)

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**Ya-Qin Zhang, IEEE Fellow**
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BY BILLY SEVEL • FAIRCHILD SEMICONDUCTOR

# Serendipity saves the day

DANIEL VASCONCELLOS

Years ago, I was a design engineer for a medical-imaging company producing MRI (magnetic-resonance-imaging) equipment. Even though I was not an RF engineer, the designs I worked on had to deal with RF-noise problems all the time, mainly within the shielded room where the magnet resided. My main responsibility was the patient-handling system, which accurately moves the patient to the point at which the scan will be the most effective. Because the RF coils in an MRI system are highly sensitive, no clocks or high-frequency-generating devices can be on in the room at the time of the scan. Well, as most engineers probably know, for many processors, there is a "sleep mode" that turns the clock off. The patient-handling system's processor entered sleep mode at the time of scan but kept the power on.

If you have ever had an MRI scan, you know that it's very loud, confining, and—more importantly to insurance companies—expensive! And if anyone must shut down an MRI system for any reason, it's quite a nuisance to the hospital or imaging center. One day, I received a call stating that the scans in one facility were full of noise, but only some of the time. I went to investigate. What could be causing this problem? Armed with the usual scopes, meters, schematics, and other tools, I kept thinking, "Great! Intermittent problem: an engineer's nightmare." I could already hear the MRI technicians explaining, "The images were horrible right before you got here, but now they're fine." Yeah, sure.

When I arrived, I asked to see the RF profile, which would show the so-called "noise" in the scans. Of course, as expected, no noise! Clean signal. However, we tried a few more coils, and the monster reared its ugly head. When I went in to manually move the patient bed, the noise appeared. I thought, "The processor should be in sleep mode." After taking apart the whole system to get to the electronics, I determined that the system clock was indeed shut off. Yet, the noise still existed! What the heck? I disconnected cable after cable to find the noise gremlin, and one tiny cable completely removed the noise. Aha! It was the cable to the optical encoder under the patient bed, which determines the 1-mm accuracy of the system positioning.

"The encoder?" I thought. But the bed isn't moving. There would be no square waves generating the harmonics necessary to interfere with the RF coils. Why is this system so noisy? I looked at the encoder signals and verified there were no pulses. So, I decided to check the 5V line. Lo and behold, there was *a lot* of high-frequency noise just on the dc power-in. The only thing I could think of was that it was a flaky internal power connection to the encoder. But there was no way of replacing or fixing it without ordering another part and then scheduling service. As I contemplated my options, I put my hands in my pockets and found an item that I had been using that day in the lab before the call: a 0.01-µF capacitor. I smiled at the tech, reached under the patient bed, and placed the capacitor over the 5V line. Poof! The noise was gone or at least gone long enough to keep the system working until someone replaced the encoder, that is.

"Serendipity" was the word of the day. The people at the imaging center were happy to see a simple solution to a frustrating problem, as was I. This solution also solved another mystery for me: why my professor in college always had diodes, resistors, and capacitors in his shirt pocket while we were all in lab! EDN

*Billy Sevel is a field-applications engineer for Fairchild Semiconductor, where he specializes in motor controls and microcontroller-based products.*

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# Floppy disks led the removable-storage stampede

RANDOM ACCESS AND CONVENIENT MEDIA MADE FLOPPIES THE MEDIA OF CHOICE IN MICROCOMPUTERS.

Before the floppy disk arrived, computer users had severely limited options for removable-storage peripherals. Paper tape found use in loading code but was far from efficient. Magnetic-tape technologies offered more capacious media but no random access. And clunky, rigid disk packs or cartridges weren't exactly portable. Moreover, all removable-storage technologies carried high prices.

Research on the floppy disk started around 1965, and, by 1975, IBM was shipping the 8-in. flavor of the venerable peripheral to load microcode into the execution units of its 370 mainframes. The random-access capabilities of the floppy would quickly usurp cassette, cartridge, paper-tape, and other removable media and become ubiquitous far beyond the IBM world.

*EDN*'s Jan 20, 1975, issue included the article "Flexible discs: a look at the latest mini-peripheral." (Read the excerpt below or access the entire article at www.edn.com/article/CA6370603.) This article described the electromechanical floppy drive. We can only guess that the prefix "mini" in the headline referred more to the minicomputers of the day than to the storage device itself.

Floppy drives would quickly move down the miniaturization curve to 5.25- and 3.5-in. versions. Moreover, capacity would escalate to hundreds of megabytes—but not quickly enough to avoid being usurped by the flash-memory drives that prevail today. EDN

01.20.75

FROM THE VAULT

## FLEXIBLE DISCS: A LOOK AT THE LATEST MINI-PERIPHERAL

WITH NO STANDARDIZATION IN SIGHT, FLOPPY-DISC USERS MUST BE WELL VERSED IN THE BASICS TO UNDERSTAND THE DIFFERENCES.

**The concept of utilizing a flexible-disc media has been present in the disc-storage-development arena for nearly a decade. Experimental work began within IBM around 1965, and it seems safe to assume that the flexible-disc concept was experimented with in several other R&D laboratories during the same time frame.**

**IBM developed a flexible-disc product in response to internal requirements for a microprogram loader for several System 370 machines. A low-cost, random-access "permanent" memory was the essential requirement. "Permanent" meant both nonvolatile and noncustomer-alterable. The result of these requirements was the IBM 23FD.**

**Since IBM was the only producer and user of flexible discs, independent peripheral suppliers that intended to compete had to follow IBM's lead. However, with OEM introduction, new applications quickly developed for the flexible-disc drive.**

**As a result, we find in today's marketplace two principal efforts in flexible-disc development: the "IBM-compatible" and the "nonIBM-compatible" drives. Product requirements exist for both drive types.**

**Specifications and performance parameters vary widely according to whether or not the flexible-disc drive is either IBM-compatible or -noncompatible. The greatest number of the companies producing flexible-disc drives uses the configuration shown in Figure 1. A lesser number of companies have in the past or are now producing flexible-disc drives utilizing significantly different configurations. Rotating contact heads, noncontact heads, and fixed-head-per-track configurations have all be implemented. Each of these offers advantages and disadvantages over the generalized configuration shown.**

**—Jan 20, 1975**

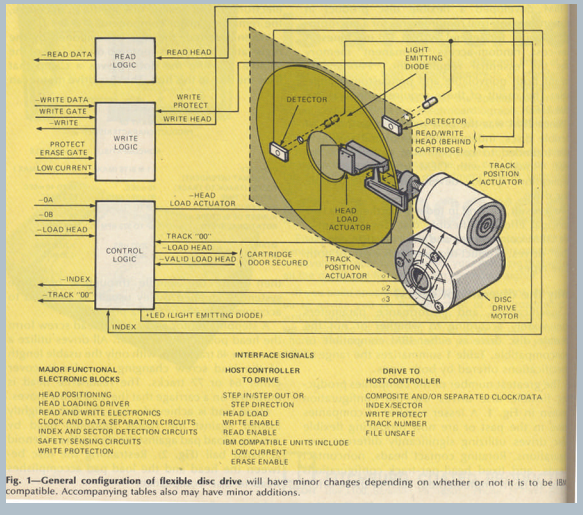


**Fig. 1—General configuration of flexible disc drive** will have minor changes depending on whether or not it is to be IBM compatible. Accompanying tables also may have minor additions.

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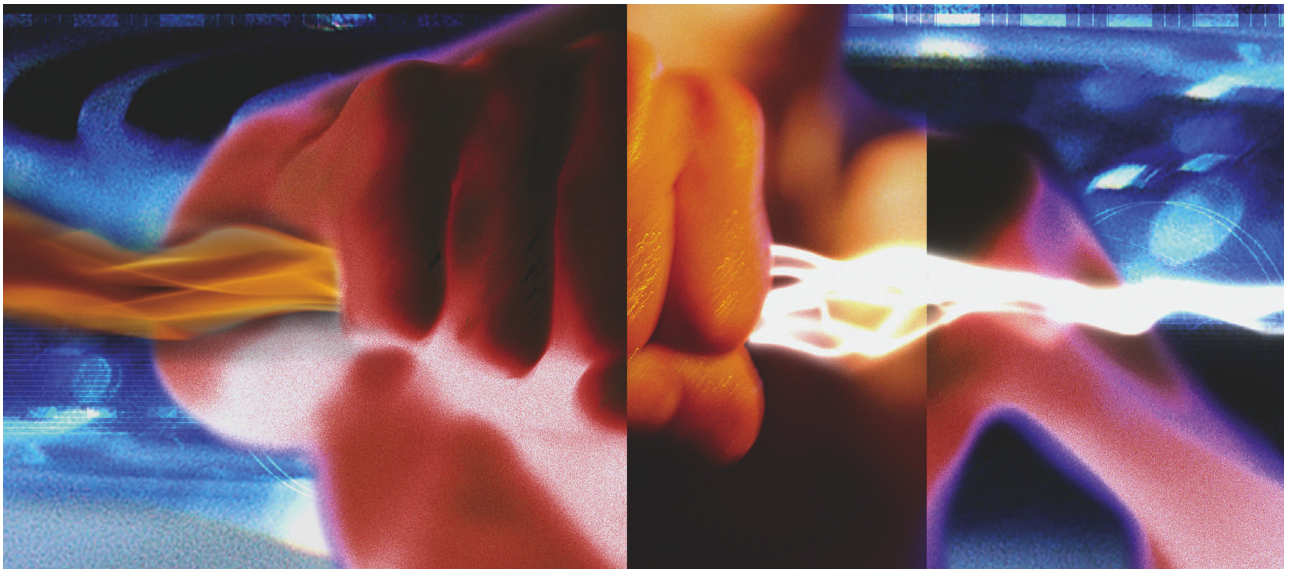

ANALOG DEVICES AND INTEL HAVE COLLABORATED ON A NEW HIGH-SPEED BUS. THE SIMPLE SERIAL TRANSPORT BUS PROVIDES PC-SYSTEM MANAGEMENT.

# HIGH-SPEED BUS FOR PC management emerges

BY CHARLES H SMALL • CONTRIBUTING TECHNICAL EDITOR

Analog Devices has teamed with Intel to develop a new serial bus that efficiently communicates computer-system heat dissipation and voltage-management and control information to safeguard the performance and reliability of high-performance desktop computers, workstations, and servers. The two companies have co-developed and launched the SST (Simple Serial Transport) bus, which enables faster and more precise communication of system temperature and voltage levels.

"Thermal management is becoming increasingly important in today's electronics applications, which are growing more complex while shrinking in size. Accurately monitoring temperature in computing products and complex cores is key to ensuring protection against malfunction or failure due to excessive heat," says Susie Inouye, research director and principal analyst with market-research company DataBeans (www.databeans.net). "Thermal-management technology allows designers to successfully monitor these complex cores that are designed on submicron geometries and continue to push the limits of heat dissipation."

By more quickly and accurately relaying this environmental information to a computer's core-logic chip set, the SST bus can dramatically reduce thermal-management errors that can lead to a drop in computing performance. "Next-generation platforms will communicate critical system information, such as temperatures, in more and varied locations within the PC platform for enhanced thermal management and reliability. Highly accurate temperature sensing enables PCs that provide a better user experience," notes Eric Ingersoll, product-marketing engineer for Intel.

## SST BUS

By communicating data in a robust, noise-immune, and scalable way, the single-wire SST bus improves on the two-wire, 100-kbps SMBus (System Management Bus) in high-performance-computing applications by offering increased bandwidth and higher noise immunity. Reducing fan noise and improving platform performance in desktop PCs, servers, and workstations, the SST bus relays key environmental information, such as temperature and

## AT A GLANCE

- The SST (Simple Serial Transport) bus enables faster and more precise communication of system-temperature and -voltage levels.
- The single-wire serial bus links sensors and south-bridge ICs.
- The new bus dramatically reduces thermal-management errors that can lead to a drop in computing performance.
- SST significantly reduces communication errors.

voltage, directly to the system's south-bridge core logic or dedicated ASIC fan-speed controllers at a rate of 1 Mbps. **Table 1** compares the SST bus to the legacy SMBus and I²C bus.

**Figure 1** shows the architecture of an SST-bus PC. The processor is an Intel Core Duo. Comparable AMD processors still use the SMBus. The SST architecture includes the MCH (memory-channel-controller) north-bridge IC, the ICH8 (I/O-channel-controller) south-bridge IC, and external thermal sensors. The ICH8 is the SST-bus host controller, and the thermal sensors are the slave or client devices. On the SST bus, a 25% duty cycle is a logic zero, and a 75% duty cycle is a logic one.

The SST bus enhances system reliability and performance by significantly reducing communication errors. In particular, when you test the buses in the same environment on new PC motherboards, the SMBus measures about one error every 10 kbits, compared with the SST bus's one error for every 1 Gbit processed. As a result, the PC user may see improved boot time and less chance of delays when the bus does not properly relay a thermal event to the core logic. In addition, the SST bus allows PC and workstation designers to use the new features, such as the recently announced Intel QST (quiet-system technology), in some next-generation Intel chip sets. With the integration of fan-speed control in the core logic, QST reduces the number of discrete fan-control components in the system, which can lower BOM (bill-of-materials) costs and allow system developers to use more programming options.

"A bus was required to enable industrywide compatibility with system-management devices, such as temperature sensors and voltage monitors in computing applications," says Steve Peterson, Intel's director of chip-set and software marketing. "Working with Analog Devices, we developed a common, robust interface that all licensed vendors can easily incorporate, allowing them to add custom capabilities, such as the Intel QST, for new environmental features in PCs, servers, and workstations."

## SMBUS AND I²C BUS

Intel's earlier system-management bus, the SMBus, is a two-wire bus similar to the I²C bus. In the early 1980s, Philips Semiconductors developed the

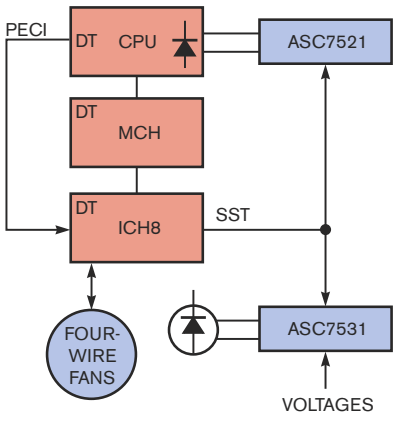


Figure 1 The architecture of an SST-bus PC includes the ICH8 south-bridge IC as the SST-bus master and the temperature sensors as slave or client devices. The ICH8 drives the PC's fans, adjusting airflow according to the temperature. The aSC7521 temperature sensor measures CPU temperature using a diode-connected transistor on the CPU. The aSC-7531 monitors five system-voltage levels in addition to measuring temperature.

I²C (Inter-IC), a simple, bidirectional, two-wire bus for efficient inter-IC control in TV sets. Philips' IC range currently includes more than 150 CMOS and bipolar I²C-bus-compatible types for performing communication functions between intelligent control devices, such as microcontrollers; general-purpose circuits, such as LCD drivers,

**TABLE 1 SST VERSUS SMBUS AND I²C**

| Parameter | Simple Serial Transport | SMBus/I²C |
|---|---|---|
| Routing and system-board noise increasing dramatically | Standard motherboard routing for non-critical traces, 5-mil-line-by-5-mil space and 4-mil-line-by-4-mil space OK | According to many motherboard designers, SMBus needs wider line and space rules in noisy areas. |
| No. of wires | Only one wire to route the bus between a host and a client | Requires a minimum of two wires: SCL and SDA. Some systems require sideband-interrupt lines, such as SMBALERT# |
| Noise susceptibility | Bit-error rate of input approximately $1\times10^{-9}$ | No published data, but testing shows results vary widely between devices. "Weakest-link" model applies |
| Speed | 2 kbps to approximately 2 Mbps | SMBus: 10 kbps to approximately 100 kbps<br>I²C: 0 to approximately 100 kbps/400 kbps |
| Intellectual property and royalties | Royalty-free Adopters License available from Analog Devices and Intel | Uncertain; contact Philips for specifics about future high-speed devices (greater than 400 kbps) |
| Data reliability | Robust methods to verify data integrity required | ACK/NAK response per byte. No further protocol required; several checksum versions are all optional |
| Conformity and compliance program | License requires that devices meet the specification. Testing plan in development | None recognized or published |

# Intersil Battery Charger ICs

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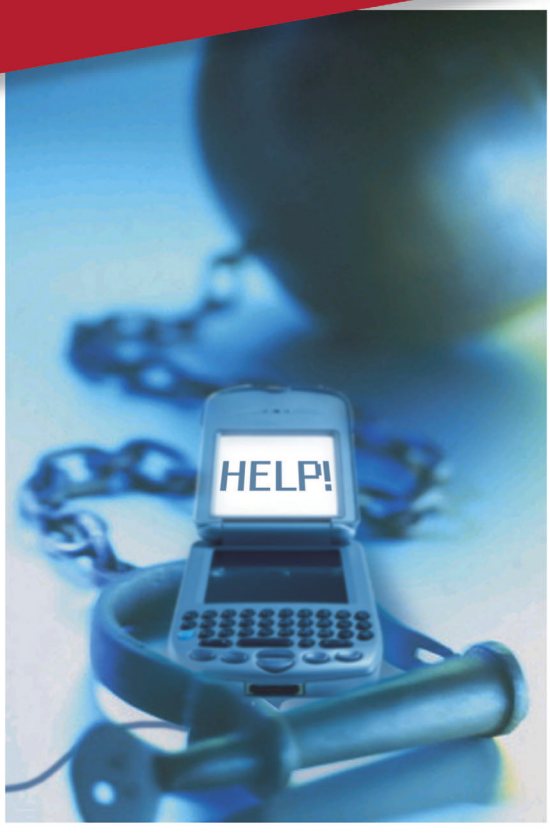
# Unshackle Your Handheld Device




## Intersil's ISL6299A is a fully integrated low-cost Li-ion or Li-polymer battery charger that accepts both USB port and desktop cradle chargers.

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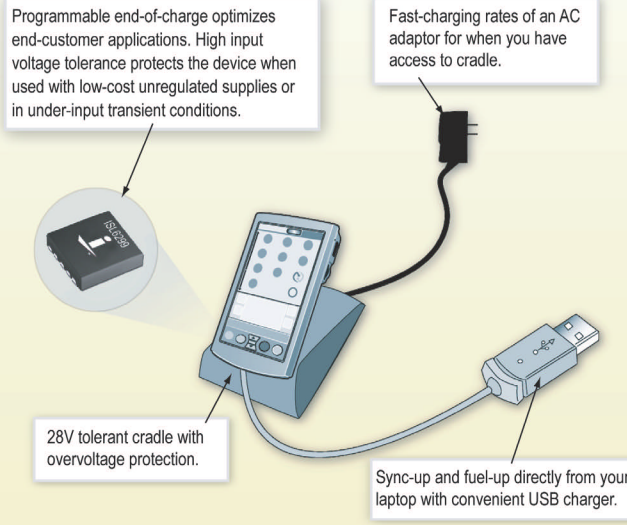
### ISL6299A System

Cradle input. The max input voltage tolerance is 28V. Programmable charge current up to 1A and programmable end-of-charge current. The included end-of-charge latch is the default input source.

USB input. Takes input from USB port or other low voltage supply. Fixed charge current at typically 380mA. Only charges when cradle source is not connected.




### ISL6299A Key Features:

- Dual-input charger for single-cell Li-ion/ polymer batteries for cradle and USB
- Low component count
- Integrated pass element
- Fixed 380mA USB charge current
- Programmable cradle charge current
- Charge current Thermaguard™ for thermal protection
- 28V maximum voltage for the cradle input
- Charge and adapter presence indicators
- Less than 0.5µA leakage current off the battery when no input power attached
- Programmable end-of-charge current with latch for cradle input
- No external blocking diode required
- RoHS compliant

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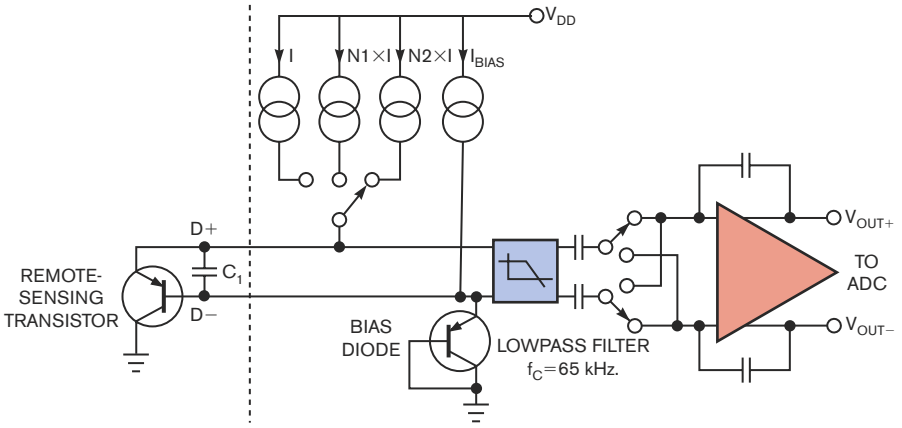
remote I/O ports, and memories; and application-oriented circuits, such as digital-tuning and signal-processing circuits for radio and video systems.

All I²C-bus-compatible devices incorporate an on-chip interface, which allows them to communicate directly with each other through the I²C bus. This design concept solves the many interfacing problems you encounter when designing digital-control circuits. I²C has become a worldwide de facto standard that is now implemented in more than 1000 ICs and is licensed to more than 50 companies.

## MEASURING TEMPERATURE

A simple method for measuring the temperature of high-performance processors and other circuitry is to exploit the negative-temperature coefficient of a diode-connected transistor by measuring the base-emitter voltage, $V_{BE}$, of a transistor operated at constant current. Unfortunately, this technique requires calibration to null the effect of the absolute value of $V_{BE}$, which varies from device to device.

Analog Devices' chips use a technique that measures the change in $V_{BE}$ when you operate the device at three different currents. In this scheme, beta compensation, the beta of a transistor varies with current. National Semiconductor pioneered beta-compensation technology and was the first to bring it to market, with the introduction of TruTherm technology in the spring of 2005. **Figure 2** shows the input-signal conditioning that the SST-bus temperature sensor uses to measure the output of a remote temperature sensor. This **figure** shows the remote sensor as a substrate transistor, which Core Duo microprocessors include for temperature monitoring, but it could also be a discrete transistor near the processor. If you use a discrete transistor, do not ground the collector and link it to the base. If the sensor is operating in an extremely noisy environment, you can add $C_1$ as a noise filter. Its value should not exceed 1000 pF. To prevent ground noise from interfering with the measurement, you do not reference the more negative terminal of the sensor to ground, but you bias it above ground by an internal diode at the D1− input (**Figure 3**).




**NOTE**: CAPACITOR $C_1$ IS OPTIONAL. USE IT ONLY IN NOISY ENVIRONMENTS.

Figure 2 The Analog Devices ADT7484 and ADT7486 measure their own internal temperatures as well as external temperatures.

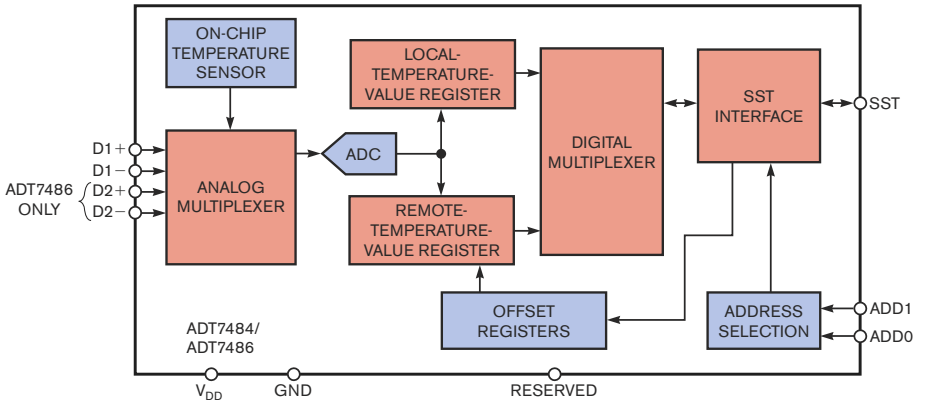



Figure 3 SST-bus temperature sensors perform beta compensation by measuring the voltage drop of a diode-connected sensing transistor using a variety of current sources, because transistor beta varies with emitter current.

## DISCRETE TRANSISTORS

If you use a discrete transistor, you do not ground the collector but instead link it to the base. If you use a PNP transistor, the base connects to the D1− input, and the emitter connects to the D1+ input. If you use an NPN transistor, the emitter connects to the D1− input, and the base connects to the D1+ input. **Figure 3** shows how to connect the ADT7484/ADT7486 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, do not reference the more negative terminal of the sensor to ground but bias it above ground by an internal diode at the D1− input.

Digital boards can be electrically noisy environments. Analog Devices advises you to take the following precautions to protect the analog inputs from noise, particularly when measuring the small voltages from a remote diode sensor:

- Place the device as close as possible to the remote-sensing diode. Provided that you avoid the worst noise sources, such as clock generators, data/address buses, and CRTs, this distance can be 4 to 8 in.
- Route the D1+ and D1− tracks close together in parallel with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
- Use wide tracks to minimize induc-

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Input Voltage


- $V_{OUT1}$: **Adjustable, 0.8V to $V_{IN}$**
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**Triple Output PWM Controller**
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- $V_{OUT3}$: **Adjustable, 0.8V to $V_{IN}$**

An adjustable overcurrent protection circuit monitors the output current by sensing the voltage drop across the lower MOSFET.

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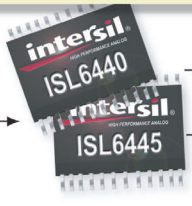


- $V_{OUT2}$: **Adjustable, 0.8V to $V_{IN}$**
- $V_{OUT3}$: **Adjustable, 0.8V to $V_{IN}$**

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- Operates from wide range of input supplies (4.5V to 24V)
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tance and reduce noise pickup. Analog Devices recommends a minimum track width and spacing of 5 mils.

- Minimize the number of copper/solder joints, which can cause thermocouple effects. If you use copper/solder joints, make sure that they are in both the D1+ and the D1− paths and are at the same temperature.
- Place a 0.1-μF bypass capacitor close to the device.
- If the distance to the remote sensor is more than 8 in., use a twisted-pair cable. This approach works for distances of approximately six to 12 feet.
- For distances as long as 100 feet, use shielded twisted-pair cables, such as Belden #8451 microphone cables. Connect the twisted-pair cable to D1+ and D1− and the shield to ground, close to the device. Leave the remote end of the shield unconnected to avoid ground loops.

**TABLE 2 SST-BUS ADDRESSES**

| ADD1 | ADD0 | Address selected |
|---|---|---|
| Low (GND) | Low (GND) | 0x48 |
| Low (GND) | Float | 0x49 |
| Low (GND) | High | 0x4A |
| Float | Low (GND) | 0x4B |
| Float | Float | 0x4C |
| Float | High | 0x4D |
| High | Low (GND) | 0x4E |
| High | Float | 0x4F |
| High | High | 0x50 |

Because the measurement technique uses switched-current sources, excessive cable or filter capacitance can affect the measurement. When using long cables, you can reduce or remove the filter capacitor. Cable resistance can also introduce errors. A 1Ω series resistance introduces about 0.5°C error.

Thermocouple effects should not be major problems because the specified 1°C resolution corresponds to about 240 μV, and thermocouple voltages are about 3 μV/°C of the temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.

## NINE SLAVE DEVICES

According to the spec sheet, you select the client address for Analog Devices' ADT7484 and ADT7486 using the address pins. The address pins connect to a float-detection circuit, which allows the devices to distinguish between three input states: high, low (ground), and floating. The address range for fixed-address, discoverable devices is 0x48 to 0x50, permitting as many as nine slave devices per SST bus (**Table 2**).

The SST bus, like Ethernet, is a networked, message-passing bus. For a summary of the commands that the ADT7484 and ADT7486 devices support when directed at the target address

that the fixed-address pins select, check out **Table 3** at the Web version of this article at www.edn.com/061026df1. The **table** contains the command name, command code, write-data length, read-data length, and a brief description.

## AVAILABLE DEVICES

Analog Devices' ADT748x family comes in eight- or 10-pin MSOPs for easy placement in areas in which space is at a premium. The ADT7484A and ADT7486A are simple, ±1°C-accurate, digital-temperature sensors that monitor their own temperature, as well as one (ADT7484A) or two (ADT7486A) remote-sensor diodes. The ADT7485A digital-temperature sensor and voltage monitor can sense its own temperature, as well as that of a remote-sensor diode. The ADT7485A can also monitor four external voltage channels and its own supply voltage using its onboard 10-bit ADC.

The Andigilog aSC7521 SST-bus remote digital-temperature sensor, accurate to ±1°C and an operating range of −40 to +125°C, measures its own temperature and that of a remote diode on the CPU or on other critical system components in which heat build-up may suddenly occur.

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The Andigilog aSC7531 SST-bus remote digital-temperature sensor and voltage monitor also measures two temperatures and adds accurate monitoring of critical system voltages. The combination of these two parts in a system plays a critical role in reporting system health with great precision to supervisory programs in Intel's high-performance chip sets. The aSC7521 sells for $1.25, and the aSC7531 sells for $1.50 (1000).

SMSC offers the EMC1102 and EMC1152. Both devices employ beta compensation to accurately measure temperature from a 65-nm processor. Each device is a dual-temperature sensor, but the EMC1152 also measures five supply voltages in desktop PCs, allowing it to monitor supply-voltage rails on the motherboard. Production samples of both the EMC1102 and the EMC1152 are available now. Prices for the parts are 90 cents and $1.20 (10,000), respectively. The EMC1102 is available in an eight-pin, "green," lead-free MSOP, and the EMC1152 is available in a 10-pin, green, lead-free MSOP. EDN

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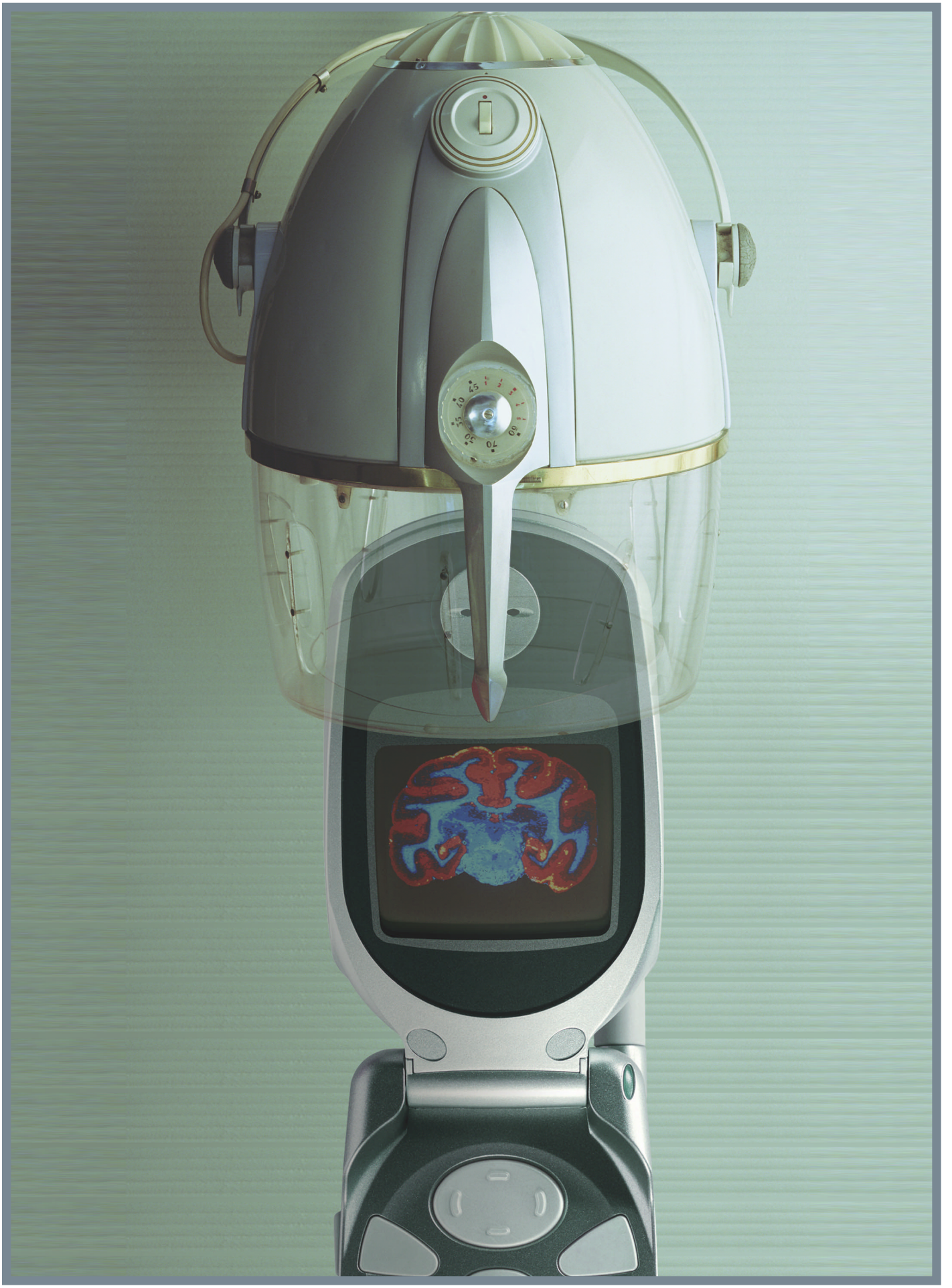
## AUTHOR'S BIOGRAPHY

*Charles H Small is a contributing technical editor for* EDN. *You can reach him at charles.small@att.world.net.*



As smart-phone sales soar, designers have their eyes on the built-in programmable graphics, growing processing power, and communications options to replace or augment one of the most challenging and expensive embedded-systems components: the user interface. With the right setup, a few clicks on a portable smart phone can connect you with and put you in charge of any embedded device. If you add special software, a smart phone can copy the look and feel of proprietary products and present a user experience similar to that of a custom embedded hardware interface at a fraction of the development cost and schedule.

## *EDN* hands-on project:

# MOBILE MAKEOVER

BY WARREN WEBB • TECHNICAL EDITOR

WITH THE RIGHT COMMUNICATIONS LINK AND READILY AVAILABLE DEVELOPMENT TOOLS, YOU CAN TRANSFORM AN OFF-THE-SHELF SMART PHONE INTO A LOW-COST, MOBILE USER INTERFACE FOR YOUR NEXT EMBEDDED-SYSTEM PROJECT.

There are plenty of applications in which a smart phone could act as a controller for embedded devices, such as industrial controllers, access-control products, medical instruments, security systems, environmental controls, and even home-automation devices. For example, MP4 Solutions offers the Airstrip OB smart-phone application, which allows obstetricians to remotely access real-time fetal-heart tracings and maternal-contraction patterns from General Electric's Centricity Perinatal information system (**Figure 1**). The smart phone's real-time display eliminates possible mistakes in interpretation by the nursing staff and allows the doctor to more frequently check on patients. The Airstrip OB supports multiple physicians accessing multiple patients and maintaining the privacy protections that the Health Insurance Portability and Accountability Act requires. Doctors pay $300 per year or $30 per month for an Airstrip OB license.

Smart-phone or converged-mobile-device technology combines PDA features, multimedia recorders and players, digital communications, and Internet access into a pocket-

sized form factor. And, by the way, these devices also make phone calls. Smart phones have virtually killed the portable-PDA market and, as they grow in processing power, are assuming many of the tasks formerly requiring a laptop computer. IDC reports that worldwide shipments of converged-mobile devices reached a record of 19.3 million units for the second quarter of 2006, marking a 1.9% sequential increase and a 42.1% year-over-year increase. IDC defines a converged mobile device as a mobile phone having a high-level operating system, such as BlackBerry, Linux, Palm, Symbian, or Windows Mobile.

## AT A GLANCE

- An off-the-shelf smart phone can replace the user-interface portion of some embedded designs to noticeably reduce the development effort.
- Although high-speed cellular data transmission is the norm, designers can also choose shorter range Bluetooth and 802.11 networks for smart-phone interfaces.
- Low-cost Web-server modules offer device manufacturers an easy way to upgrade embedded devices for compatibility with smart phones.
- Integrated development tools from most handset vendors ease the custom programming necessary for smart-phone user-interface design.

## FLEXIBLE PHONES

Smart phones offer embedded-system designers a number of benefits over custom hardware. In addition to the obvious cost and size advantages, smart phones offer design flexibility. A single smart phone can control multiple embedded devices, and, conversely, multiple authorized users can control a single embedded device. Depending on the capabilities of the embedded system and the phone, users can exchange wireless data over short-range technologies, such as infrared or Bluetooth; medium-range 802.11 networks; or long-range cellular systems. Yet, smart-phone adoption brings plenty of problems with it. For example, security and privacy concerns may significantly complicate the software. Also, each user requires a smart phone with application software and data service. Smart phones are available with a variety of form factors, screen sizes, processor speeds, and operating systems. This range of choices allows users to select the exact performance they need but creates integration and interoperability problems for embedded-system designers. Finally, in most large enterprises, the information-technology department dictates cell-phone policy and carrier selection.

Most smart phones operate on CDMA (code-division-multiple-access) or GSM (Global System for Mobile communications) cellular networks. With CDMA, the frequency of the transmitted signal hops according to a defined code, and only a receiver following the same set of frequencies can detect it. CDMA permits many radios to share the same frequency channel. GSM is the most popular cellular standard: More than 2 billion people in more than 200 countries use it. Most cellular technologies have a third-generation evolution path to extend data rates for high-bandwidth-system applications. Examples are EDGE (enhanced data rates for GSM evolution) and EV-DO (evolution-data optimized).

Several ways exist for interfacing a smart phone with an embedded device over an available communications link. The basic design challenge is to integrate communications hardware and software into the embedded device and possibly develop a custom application for the handset. A popular approach is to add Web-server features to the embedded device to incorporate Internet connectivity. If the embedded product has surplus processing power and a communications port, designers can add Web-server software directly into the firmware. For example, the open-source, small-footprint AppWeb Web server aims at embedded devices and applications. The software is licensed under the GNU open-source license, and a community of developers sup-


Figure 1 MP4 Solutions' Airstrip OB smart-phone application offers obstetricians remote access to real-time fetal-heart tracings and maternal-contraction patterns.

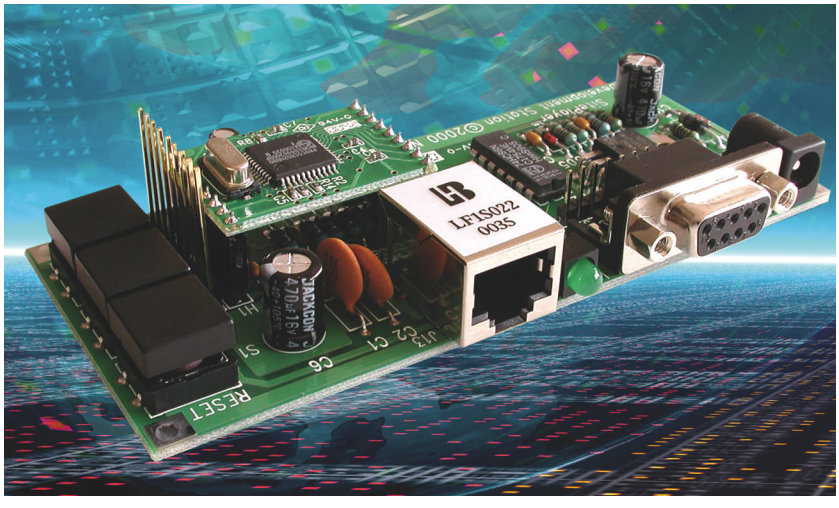
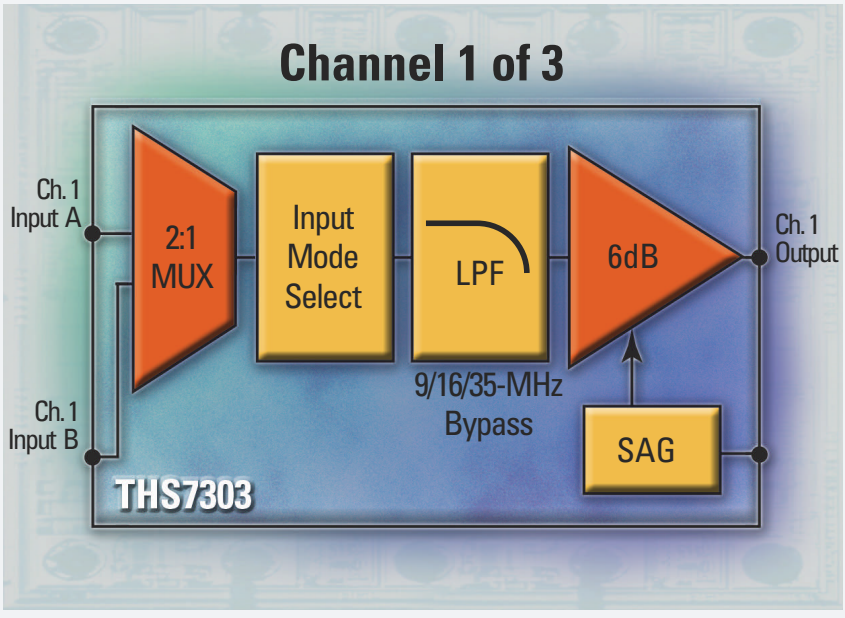



Figure 2 NetMedia's $100 SitePlayer developer's kit features a Web server, a 10BaseT Ethernet controller, flash Web-page memory, a graphical object processor, and a serial-device interface.

# 3-Ch. Low-Power Video Amp with I²C Control

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|---|---|---|---|---|---|---|---|---|---|
| THS7303 | 3 | 9, 16, 35 | 5 | 190 | 6 | AC-Bias, AC-STC, DC, DC+Shift | AC or DC | Yes | $1.65 |
| THS7313 | 3 | 8 | 5 | – | 6 | AC-Bias, AC-STC, DC, DC+Shift | AC or DC | Yes | $1.20 |
| THS7353 | 3 | 9, 16, 35 | 5 | 150 | 0, Adjustable | AC-Bias, AC-STC, DC, DC+Shift | AC or DC | No | $1.65 |

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ports it. It provides a standards-based, dynamic Web-page-creation environment. You can download the free AppWeb software with full source code at www.appWebserver.org.

To retrofit products with limited expansion capability, you can opt for a drop-in Web-server module that includes a serial interface to your embedded product on one end and an Ethernet interface on the other. The Web server includes networking software, leaving the designer free to concentrate on the embedded-system application. The $30 SitePlayer module from NetMedia and the $50 Xport embedded-Ethernet-device server from Lantronix are examples of add-on Web servers. Each device allows you to create smart-phone-compatible Web pages using standard HTML (Hypertext Markup Language)-authoring tools and download them directly to built-in flash memory. You can then communicate with and control the device from any standard or smart-phone browser.

## SHORT LINKS

Short-range wireless links, such as infrared, Bluetooth, and Wi-Fi, can also provide the connectivity necessary to control or monitor an embedded device. Many smart phones offer built-in Bluetooth transceivers to wirelessly link to nearby devices, such as headsets, GPS (global-positioning-system) modules, other smart phones, and PCs, for synchronization. With an embedded device that integrates a Bluetooth transceiver for a custom smart-phone application, you can establish a user interface for short-range, interactive applications. You can establish a similar communications link over the infrared channel, but alignment is sometimes tricky, depending on sensor placement. Although Wi-Fi transceivers would provide a longer range connection, smart-phone carriers hesitate to include the capability because a VOIP (voice-over-Internet Protocol) connection could bypass their per-minute charges.

Although you can launch an embedded user interface by simply selecting the Web server's address through the smart phone's browser, a few software modifications create a more customized look and feel and simplify the process. Most

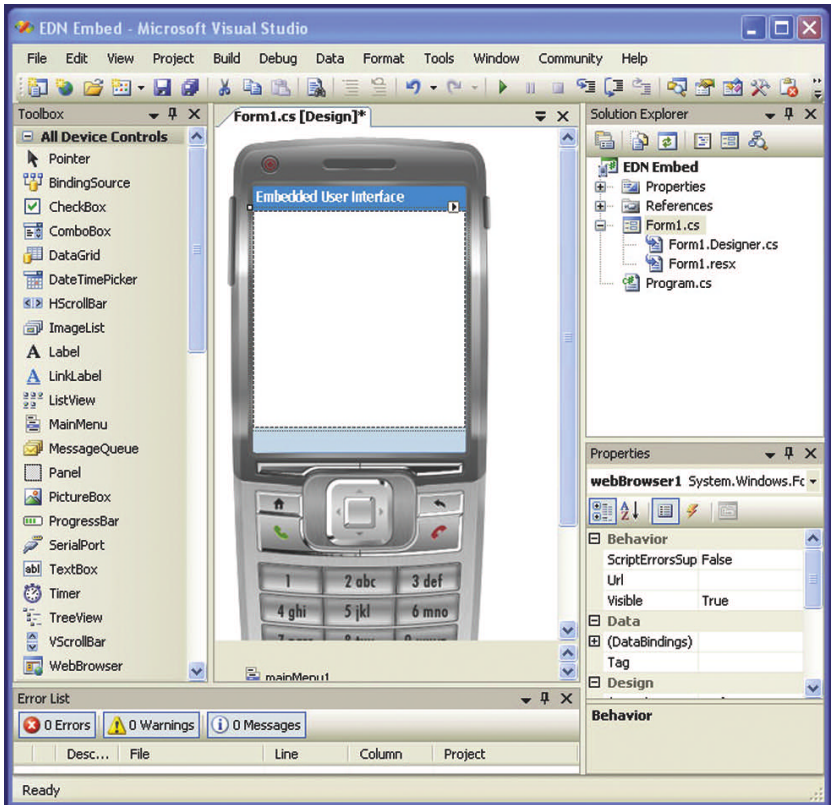


Figure 3 The Microsoft Visual Studio environment with the Windows Mobile developer's-resource-kit option delivers drag-and-drop smart-phone programming.

smart-phone vendors provide development tools to encourage third parties to develop software add-ons, increasing handset sales or extending per-minute charges. Although embedded devices in general use a wide array of software vendors plus in-house custom software, smart-phone software comes from very few sources. Operating systems, such as embedded Linux, and systems from Symbian, Windows Mobile, Palm, and Research in Motion account for most smart-phone platforms.

A large group of cell-phone manufacturers, including Nokia, Ericsson, Sony, and Samsung, own and support Symbian, which has the largest smart-phone market share. The Symbian OS includes a real-time, multithreaded, pre-emptive kernel and supports most telephony, messaging, and multimedia protocols. The developers of Symbian designed it for handheld devices, and it had limited resources and a strong emphasis on conserving memory and power. Symbian offers a complete set of development tools, including both paid and free versions, on its Web site.

The Palm-operating-system-development tools are more mature than those from any other smart-phone-software supplier, but the company has split, creating some confusion among developers. PalmOne is the hardware spin-off of Palm, and PalmSource, which Access recently acquired, maintains the Palm operating systems and works with third-party developers. Application developers can choose from C, C++, Visual Basic, or Java programming languages plus the Freescale CodeWarrior or Eclipse integrated development environments. You can find development tools, documentation, and tutorials at the PalmSource Web site.

Linux, the fastest growing operating system for smart phones, provides developers with open-source code, freedom from licensing restrictions, free development tools, and a huge support community. Supporting this rapid growth, a spokesman recently announced that

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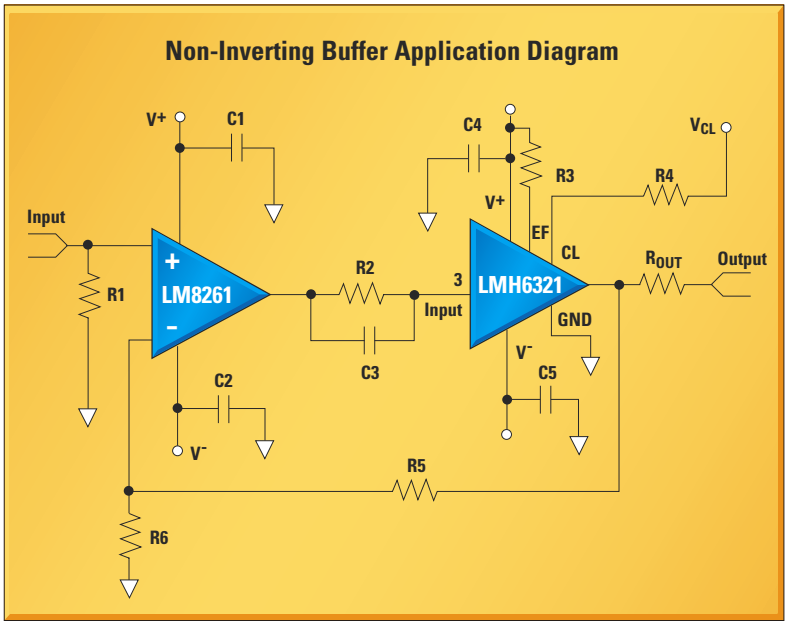


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Linux will power more than half of the mobile phones that Motorola ships within two years. Evans Data Corp (www.evansdata.com) reports that almost one-quarter of all smart phones sold in 2005 used the Linux operating system. However, Linux has some problems. Critics claim that Linux smart-phone platforms suffer from fragmentation and interoperability issues due to the ease with which developer groups can modify their code. The LIPS (Linux Phone Standards) Forum and the OSDL (Open Source Development Labs) have recently teamed up to define standards that promise to turn Linux into a plug-and-play mobile-phone platform.

## WINDOWS TO GO

To support its latest operating software for Pocket PC and smart-phone devices, Windows Mobile 5, Microsoft revamped its tool structure and designated Visual Studio 2005 as the main integrated development environment for building all Windows mobile applications. Developers have a language choice of C++, C#, and Visual Basic, plus an expanded set of application-programming interfaces for mobile devices. Visual Studio 2005 also provides device emulators to simulate application-software operation directly on the PC workstation. You can find a detailed overview of Microsoft's tools, tutorials, and sample applications at the Windows Mobile Developer's center at www.microsoft.com/windowsmobile/developers.

Since I have access to a fairly new Motorola Q smart phone based on the Windows Mobile 5 platform, I decided to use it to create a basic user interface to monitor and control a simple embedded device. The Motorola Q includes a 320×240-pixel display, a full QWERTY keyboard, EV-DO support, integrated Bluetooth, a speakerphone, a 1.3 million-pixel camera, and extensive multimedia features. With a built-in Web browser and e-mail capability, the Q has all the communications functions necessary to serve as an embedded user interface.

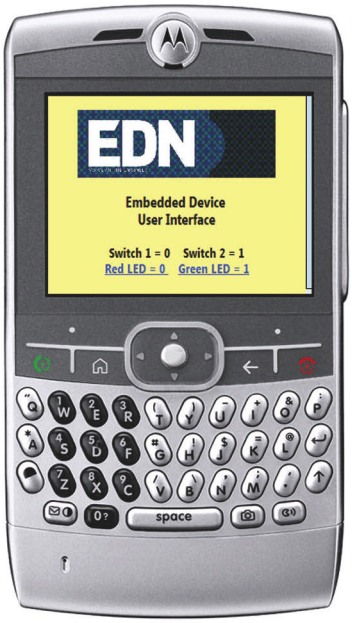


Figure 4 This emulator image for the Windows Mobile 5 allows designers to realistically simulate and interact with Motorola Q smart-phone applications.

My first task was to locate the development tools necessary to create custom applications for the Q. I started at the Microsoft-developer Web site to download the smart-phone SDK (software developer's kit) and a 90-day trial copy of Visual Studio 2005. As soon as I discovered that the combined download was nearly 3 Gbytes, I coughed up the $13 to have Microsoft deliver the DVDs by mail and prepared for a long wait. I was surprised to find the package from Microsoft in my mailbox in just two days. Installation was straightforward, and I was able to test some sample applications within a few hours. I then ventured to the Motorola developer Web site, where I found the Q developer guide with instructions for installing the company's custom emulator image into Visual Studio 2005.

Now, with a complete development environment for Motorola Q, I needed an embedded system to control. Luckily, I had on hand a developer kit for the SitePlayer Web server that could simu-

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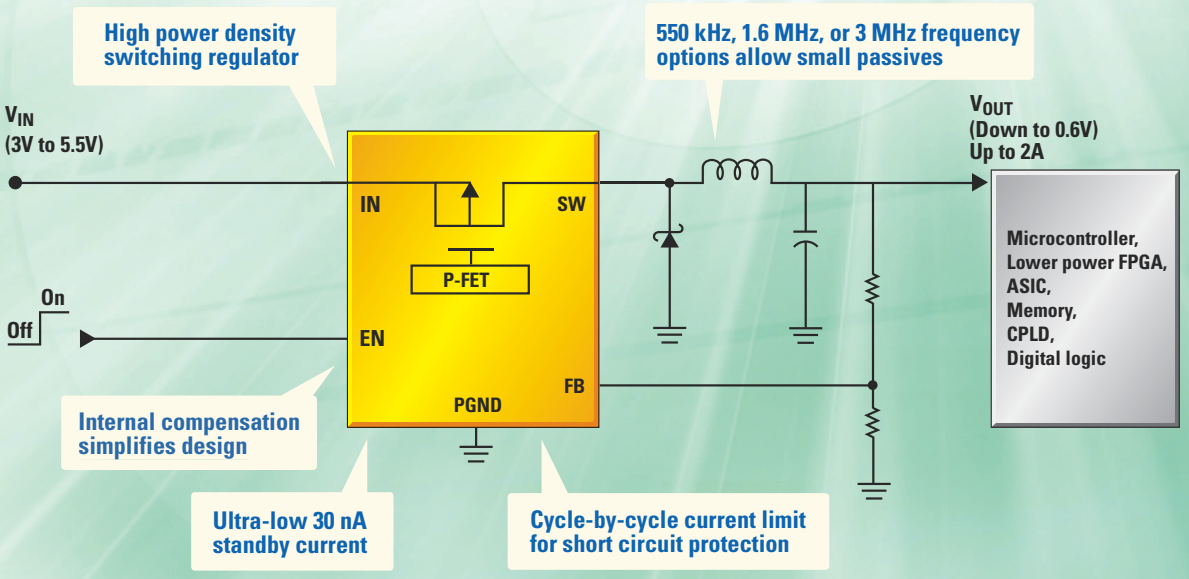


| Product ID | $I_{OUT}$ | Packaging |
|---|---|---|
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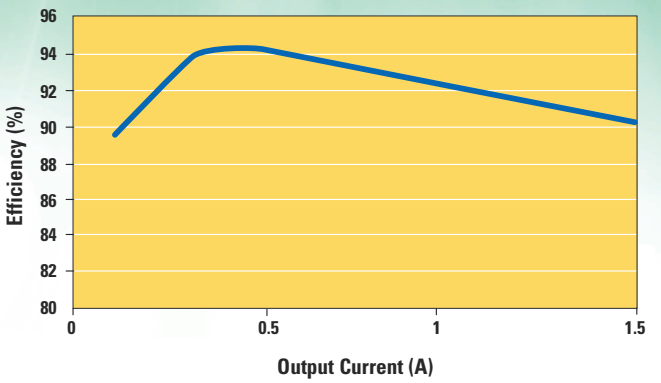



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late a rudimentary embedded device. The $100 kit includes a host board with LEDs and switches, a temperature sensor, and a SitePlayer module (**Figure 2**). The kit also includes sample software and a library of graphical knobs, switches, LEDs, and other user-interface tools to aid in Web-page development. With a serial connection to my laptop and an Ethernet link into my home network, I could interact with the sample Web pages preloaded into the SitePlayer. I could control two LEDs and read the state of two switches from the development kit with my standard browser pointing to the SitePlayer's factory-set IP address.

## WEB VIEW

To create custom Web pages to download to the SitePlayer, I needed an HTML-authoring tool that could modify the sample code that NetMedia provides. With a quick Google search, I found and downloaded the free Nvu (new view) Web-authoring system. Nvu allows WYSIWYG editing of pages without dealing with the HTML structure and has features similar to those of Microsoft's FrontPage and Adobe's Dreamweaver. After a short learning process, I was able to load the sample pages, retain the hardware hooks, and create all new pages tailored to the small smart-phone graphical display. The open-source Nvu system is available under the Mozilla public license.

The final step in the process was to create a special smart-phone application for the Motorola Q that would bypass the normal Web-address-navigation details and directly display the user-interface page from the SitePlayer when I invoked it. At first, I was expecting a huge learning curve, given the tools and features built into Visual Studio and the Compact Framework details for Windows Mobile 5. However, after watching a few of the online tutorials from the Microsoft developer's site, I found that my application was simple and required only a single line of code to identify the URL of the SitePlayer. With the smart-phone SDK installed, I could drag and drop my control, the WebBrowser, onto the simulated display, add my line of code, build the object code, and deploy the result onto the Motorola Q emulator directly from the Visual Studio programming environment (**Figure 3**). OK, maybe it wasn't as simple as it sounds. I had problems deciphering the device controls, connecting the emulator to my network, and formatting the Web pages for the 320×240-pixel display.

Although the application turned out to be simpler than I had first envisioned, I was able to turn the LEDs on and off from the application by selecting the appropriate link and clicking the center of the five-way switch on the smart-phone emulator (**Figure 4**). The system could also display switch settings, although not in real time. The way that I wrote the application required a page refresh to read the current switch states—probably not acceptable to the marketing folks. Notwithstanding the tiny shortcomings in my application software, the smart-phone user-interface concept has enormous potential to reduce the cost and schedule for embedded-system projects. EDN

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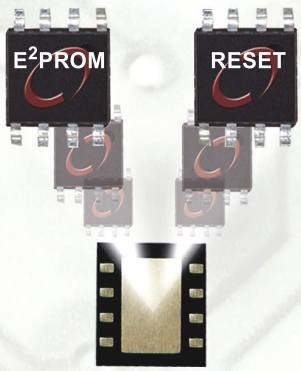


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| CAT811/CAT812* | Single | Yes | | | SOT-143 |
| CAT1232LP/1832* | Single | Yes | Yes | | DIP, SOIC, MSOP |
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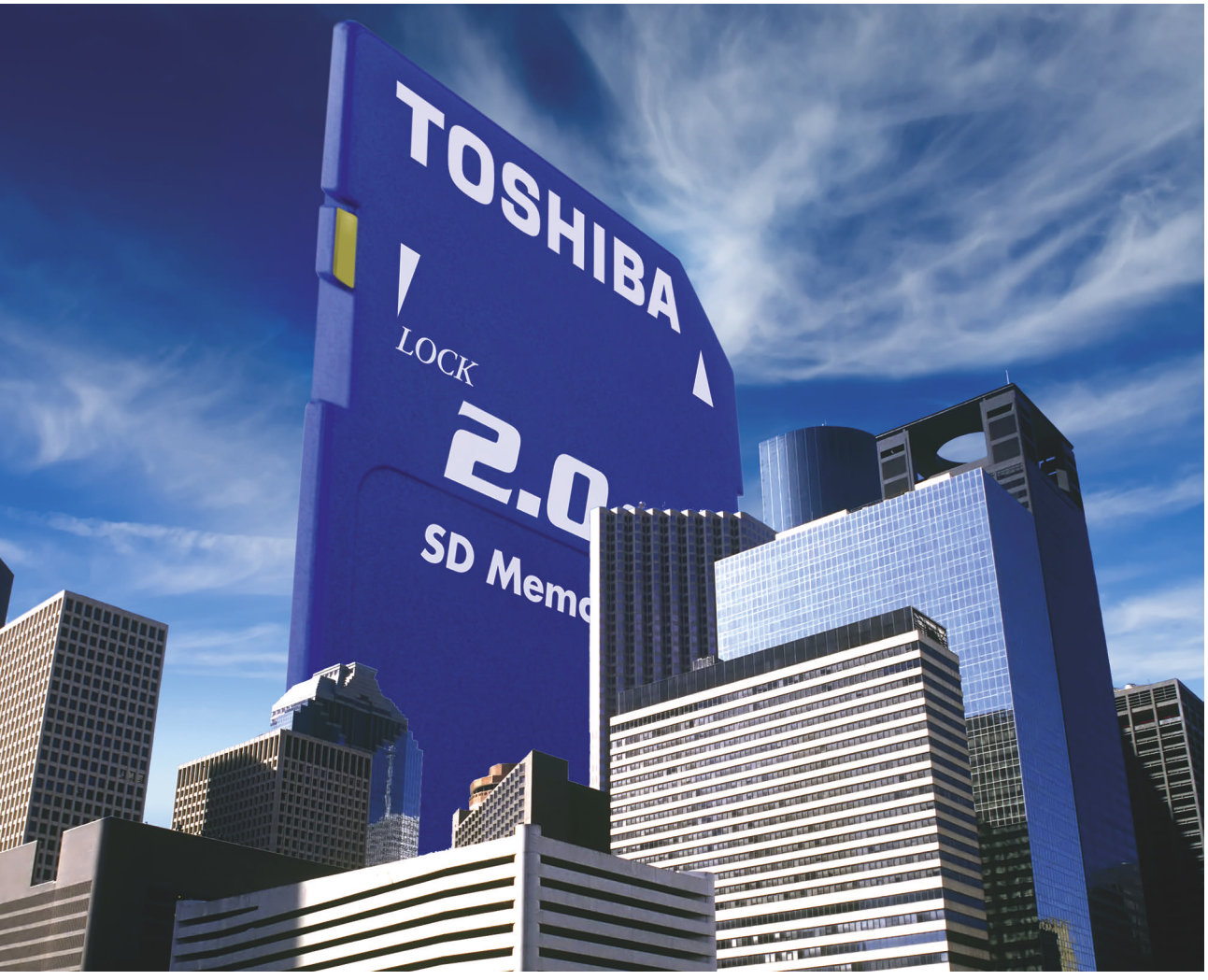


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# Handling differential skew in high-speed serial buses

DIFFERENTIAL SKEW HAS BECOME A PERFORMANCE-LIMITING PHENOMENON. YOU CAN MANAGE IT WITH A VARIETY OF APPROACHES.

Until recently, wide synchronous buses were the method of choice for high-data-rate digital communications because digital logic could not support the switching rates for required bandwidth on a single lane. Unfortunately, wide synchronous buses become problematical at high clock rates. As speeds increase and buses become wider, it becomes increasingly difficult to obtain required setup-and-hold times on all the lines in a wide bus. These facts have driven the use of very-high-bit-rate serial buses with embedded clocks. Embedded clocks are implicit in serial buses, and the clock frequency is 1/UI (unit interval) of data change. This article assumes an 80-psec UI and, therefore, a 12.5-GHz clock frequency (**Figure 1**).

A little-regarded phenomenon, differential skew, has become a fundamental performance-limiting issue for high-speed serial-communications links. "Differential skew" refers to the time difference between the two single-ended signals in a differential pair. The operation of such links involves significant amounts of signal processing to recover clocks, reduce the effects of high-frequency losses, reduce ISI (intersymbol interference), and improve SNR. Skew limits the bandwidth of these links, adds data-dependent jitter, and limits the possibility of equalizing links to compensate for high-frequency skin effect and dielectric losses.

Skew arises from a variety of sources. The most common and universal cause of skew is the difference in the effective lengths of the two transmission lines in the lane connecting a transmitter to a receiver (**Figure 2**). **Figure 3** illustrates the effects of that skew. The right side of **Figure 3** represents the skew in the differential signal. The small amount of skew in **figures 2** and **3**, about 0.2 UI, or 16 psec, can result from a length difference of less than ⅛ in. (3 mm).

You can add various amounts of skew to a sophisticated analog FIR-filter equalizer (**Figure 4**). **Figure 5** shows the simulated effects of adding this skew. This filter equalizes the frequency-dependent loss of dielectrics, which predominates in pc-board interconnects at frequencies of 5 GHz and greater. For the zero-skew-input case, the 12-UI burst exhibits its minimum ISI and maximum output amplitude, and, with small amounts of skew, both the ISI and the output amplitude degrade significantly.

Even perfectly matched lengths do not guarantee zero skew. Many media—from cables to pc-board materials—have nonuniform dielectric constants, which can cause skew in perfectly matched path lengths as short as a few inches. A prime example is fiberglass-reinforced epoxy, such as G10. In this case, the dielectric constant of the fiberglass differs from that of the epoxy, and the fiber bundles are spaced at a distance that is comparable to the width of conductors in stripline or microstrip interconnects. Random placement of the fiberglass bundles with respect to the location of the conductors on the pc board results in uncontrolled differential skew. This skew can be as large as 25 psec in 4 in. (10 cm) of interconnect (**Reference 1**).

## NEW SOLUTIONS

You can correct differential skew by improving control of the manufacturing process to reduce the variation of effective dielectric constant as a function of location. You could use irregular angular relationships between the direction of the fiber bundles or other causes of anisotropic dielectric con-

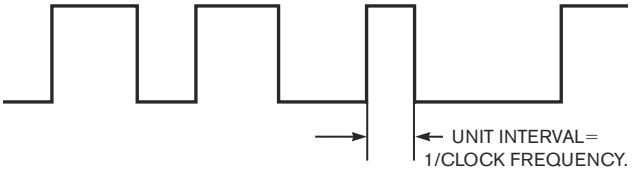



Figure 1 This article assumes an 80-psec UI and, therefore, a 12.5-GHz clock frequency.

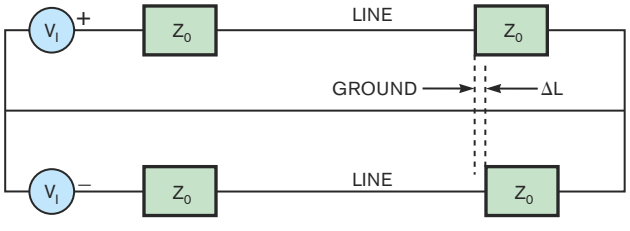



Figure 2 The most common and universal cause of skew is the difference in the effective lengths of the two transmission lines in the lane connecting a transmitter to a receiver.

stants and the conductors in the lanes. If each conductor of length L crosses the same number of fiber bundles, the delay associated with each conductor should be the same. Alternatively, you can measure the skew and replace a conductor link with a link containing the inverse of the measured amount of skew—an expensive proposition. Creating a library of precisely known differential delays involves a significant amount of test time, and it requires the accurate assembly, measurement, and cataloging of many cables or other forms of interconnect.

Another, more promising, approach is to detect differential skew and adjust the delay in one, the other, or both paths to reduce the skew to near zero. This approach involves detecting the skew and then adjusting the delay.

## DETECTING SKEW

Modern oscilloscopes have timing resolutions of 1 psec or less, but connecting an oscilloscope to the differential inputs of a receiver IC can typically introduce systematic skew of 2

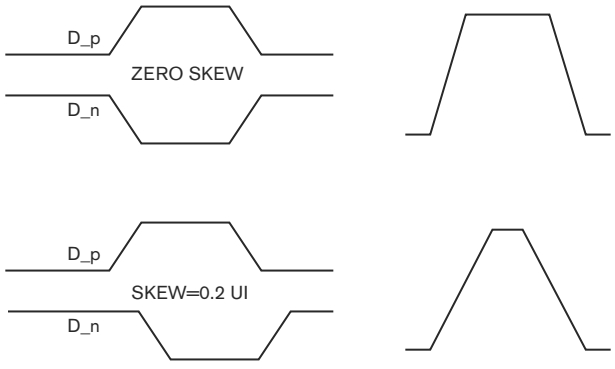



Figure 3 A small amount of skew, about 0.2 UI, or 16 psec, can result from a length difference of less than ⅛ in. (3 mm).

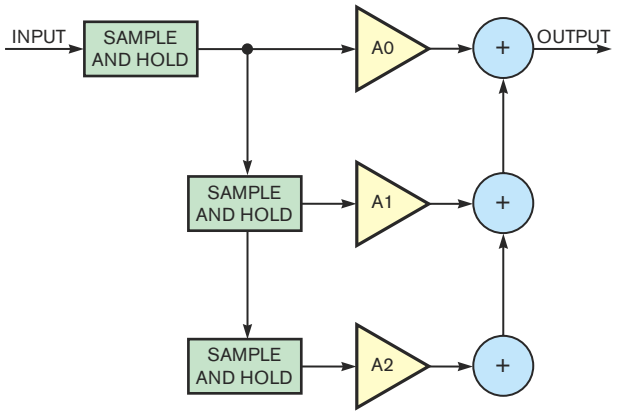
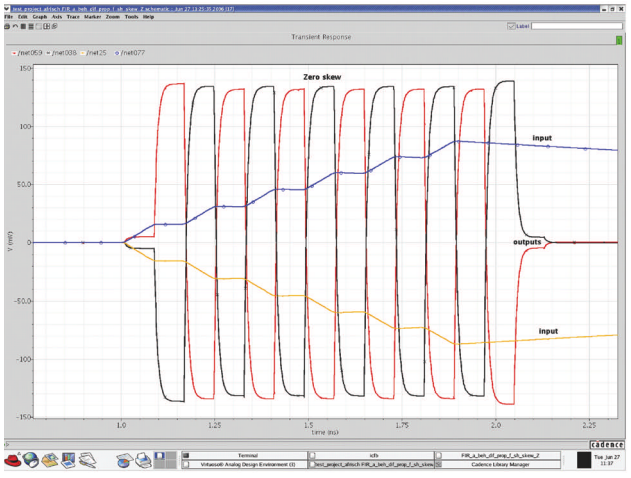
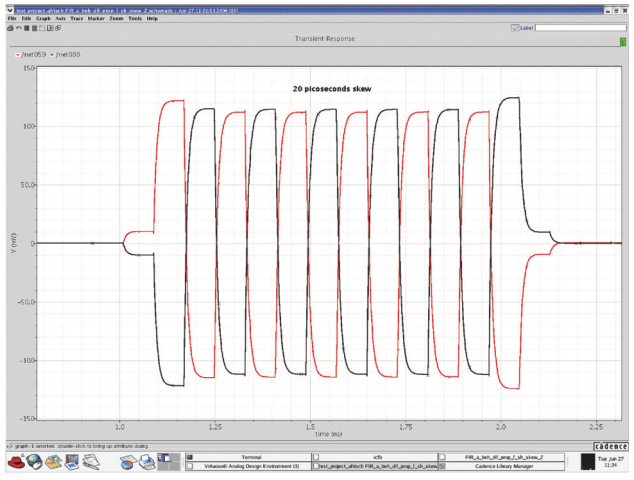



Figure 4 You can add various amounts of skew to a sophisticated analog FIR-filter equalizer.




(a)

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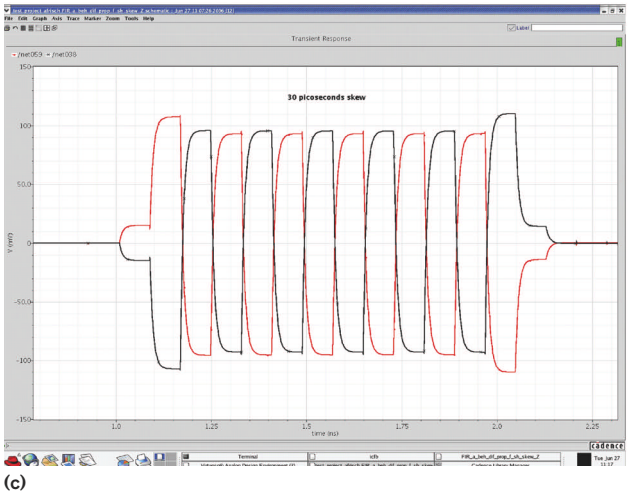


(c)

Figure 5 For the zero-skew-input case (a), the 12-UI burst exhibits minimum ISI and maximum output amplitude. With small amounts of skew, such as 20 psec (b) and 30 psec (c), both the ISI and the output amplitude degrade significantly.

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or 3 psec. Uncertainties associated with the probe positioning, the location of the ground connections, and the differences between the load impedances of the two probes cause this skew. US Patent 6,909,980 describes a method for

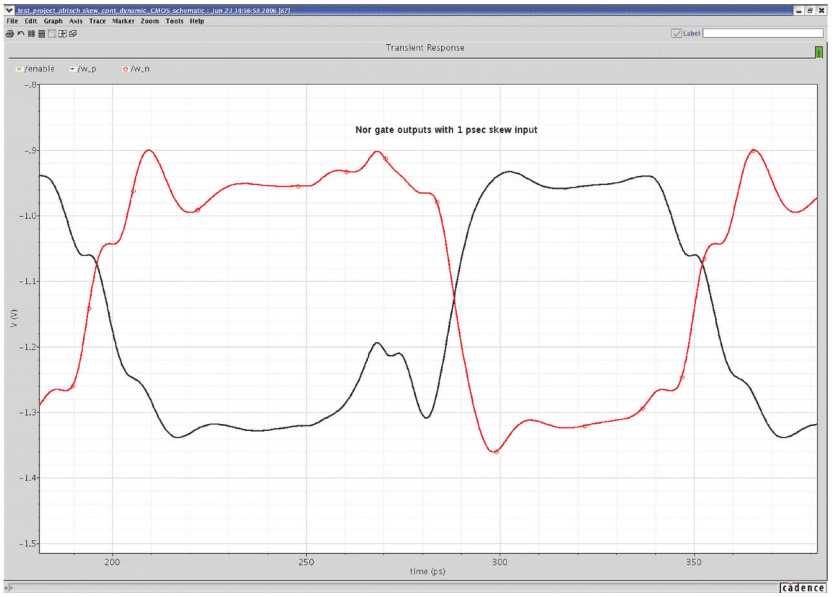


Figure 6 A circuit-level simulation for a system having 1 psec of skew shows that, at 50% duty factor, the skew is zero, so 1 psec of skew is easily detectable.

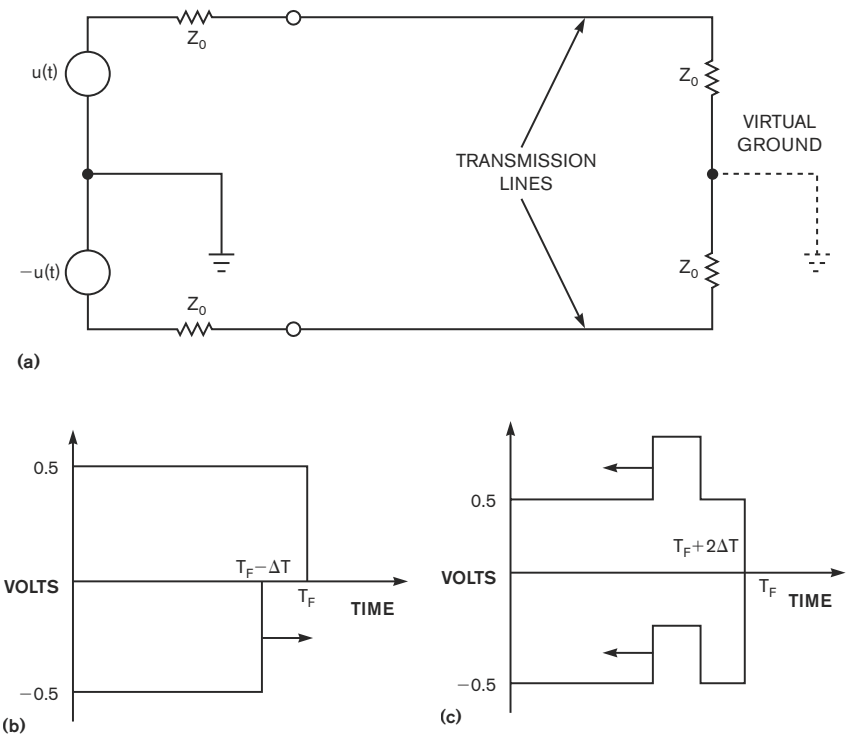


Figure 7 The reflections are easy to detect at the transmitter (a), and they indicate not only the presence of skew, but also which of the two signals arrived at the receiver first (b) and which arrive later (c).

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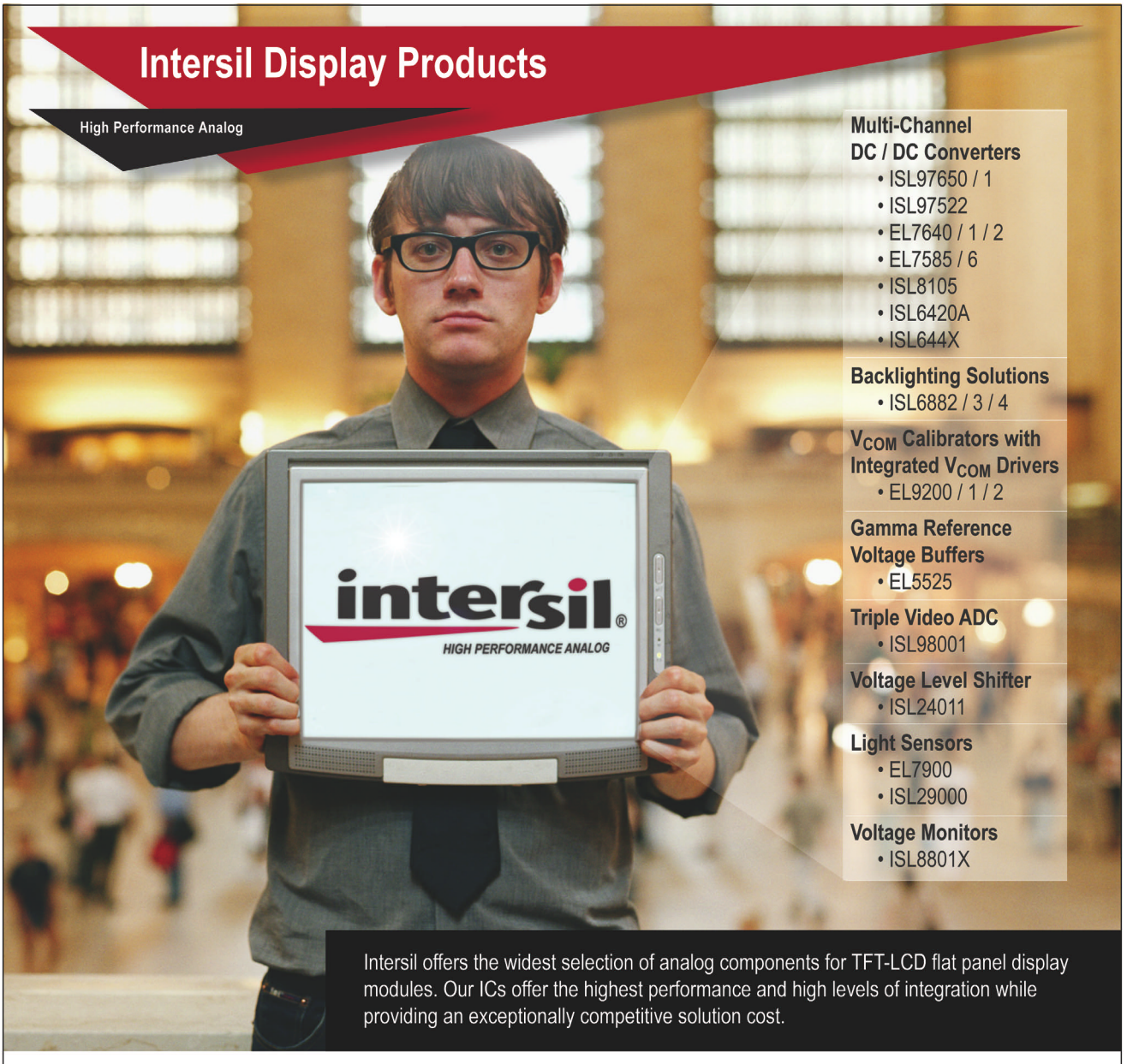


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deciding how a piece of test equipment should adjust the timing of input differential signals to obtain optimal skew values in an eye diagram (**Reference 2**). The patent uses independently programmable "paired independent skew circuits" for the true and complementary versions of a differential input, thereby letting you deskew the signal circuit. The patent assumes that the differential skew arises as a consequence of problems in the interconnection to the test equipment. The invention does not deal with skew introduced by interconnection between a source and the input circuit of a remote IC that is not a part of such test equipment. The patent gives a good approach for displaying eye diagrams, not for measuring skew.

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**IF THE REQUIRED SKEW RESOLUTION IS SEVERAL PICOSECONDS LONG, THE SKEW ADJUSTER CAN INSERT ACTIVE DELAY INTO A PATH USING A MULTIPLEXER.**

Observe the received signals inside the receiver. You can determine the skew with a NOR latch. If there is no skew, the average value of the output waveforms from Q_p and Q_n will be the same. Any skew adds to the average value of one waveform and subtracts from the average value of the other waveform. This situation makes it easier to detect small amounts of skew. **Figure 6** shows a circuit-level simulation for a system having 1 psec of skew. At 50% duty factor, the skew is zero, so 1 psec of skew is easily detectable.

Observe the reflection from the input of the receiver. If the receiver is differentially terminated, the virtual center of the termination is at ac ground when no skew exists. When skew exists, large reflections launch at the receiver during the skew interval. The first signal to arrive at the line-to-line termination "sees" the value of that termination resistor in series with the characteristic impedance of the transmission line that connects to the opposite side of the termination resistor. During the skew interval, the termination appears to be $3\times Z_N$ instead of $Z_N$. This fact results in a reflection coefficient of $(Z_T-Z_N)/(Z_T+Z_N)=(2\times Z_N)/(4\times Z_N)=0.5$. This large reflection coefficient persists until the arrival of the second signal at the end of the skew interval. At that time, the voltages at the opposite ends of the termination resistor are equal and opposite in sign. So the line-to-line termination has the same effect as two resistors, each of value $Z_N$, providing ideal terminations to the two lines.

The reflections are easy to detect at the transmitter, and they indicate not only the presence of skew, but also which of the two signals arrived at the receiver first. **Figure 7** shows the model for the skew detector and the corresponding waveforms. It's important to note that, in this case, the indicated skew could be the result of some transmitter skew and some interconnect skew, but the skew-detection method determines the final resulting skew, no matter where the contributions came from. (I have filed a patent application in this area.)

## ADJUSTING SKEW

If the required skew resolution is several picoseconds long, the skew adjuster can insert active delay into a path using a multiplexer. This time-tested and proven methodology is largely in the public domain. For skew requirements of approximately 1 psec or less, you can use an interpolator to interpolate between two fixed delays whose difference is approximately 10 psec. Many timing interpolators are in the public domain. For smaller target amounts of skew requiring subpicosecond resolution in the timing adjuster, a programmable-delay line using current control or varactors is a good choice. Patent applications exist for this type of system.

Resolving small amounts of skew is not

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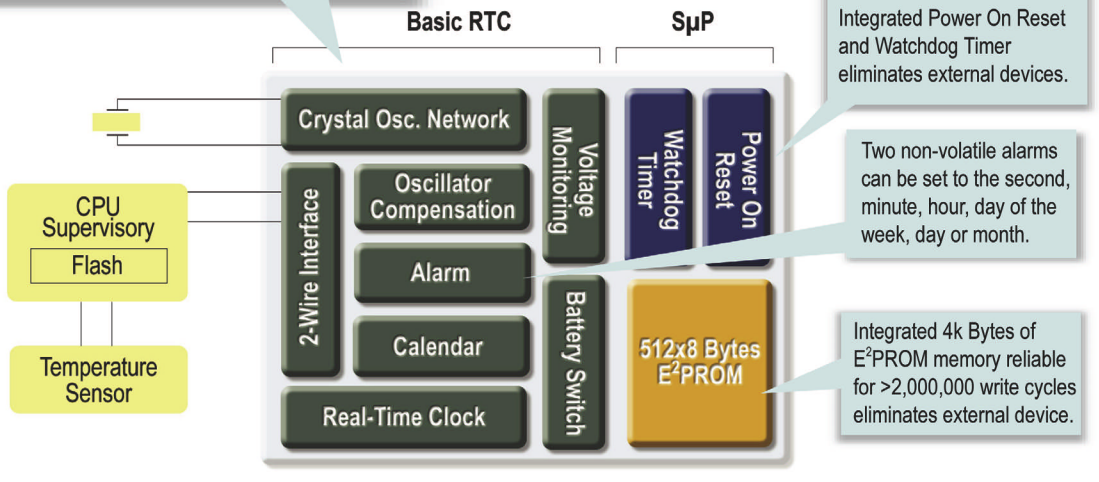


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|---|---|---|---|---|---|---|---|---|
| ISL12026 | 512 X 8 | 2 | N | N | $\overline{IRQ}$/FOUT | | 5 Sel. (2.63V to 4.64V) | 8-Ld SO/TSSOP |
| ISL12027 | 512 X 8 | 2 | Y | Y | $\overline{RESET}$ | | 5 Sel. (2.63V to 4.64V) | 8-Ld SO/TSSOP |
| ISL12028 | 512 X 8 | 2 | Y | Y | $\overline{IRQ}$/FOUT | | 5 Sel. (2.63V to 4.64V) | 14-Ld SO/TSSOP |
| ISL12029 | 512 X 8 | 2 | Y | Y | $\overline{IRQ}$/FOUT | | 5 Sel. (2.63V to 4.64V) | 14-Ld SO/TSSOP |

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**ENSURING THAT THE SKEW EXISTS AND IS NOT AN ARTIFACT OF THE MEASUREMENT IS MORE DIFFICULT THAN RESOLVING SMALL AMOUNTS OF SKEW.**

too difficult. Ensuring that the skew exists and is not an artifact of the measurement is more difficult. Two paths typically exist between the device under test and the measurement device. One connects each of two points whose differential skew you are determining to corresponding inputs of the measurement device or skew detector. If these paths have a differential delay, an error will appear in the measurement result. If the two paths have different rise times or bandwidths, a differential delay will result. If the measurement device is an oscilloscope that uses a probe for each input, the skew of the probes, their cables, and the difference in their rise times can cause a significant amount of skew.

Also, when measuring the relative duty factors of the output of a latch-based skew detector, bias or leakage current in the input of the dc amplifier can cause significant errors. **EDN**

## AUTHOR'S BIOGRAPHY

*Arnold Frisch is principal of intellectual-property vendor WarpSpeed Chips LLC (Portland, OR) and a member of the technical staff at automated-test-equipment manufacturer Credence Systems Corp (Milpitas, CA, www.credence.com), where he designs mixed-signal ICs and systems. He has a bachelor's degree in electrical engineering from the City College of New York and a master's degree in electrical engineering from the Brooklyn Polytechnic Institute. He enjoys playing golf with his wife and friends, exercise, history, and family.*

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# For These Amplifiers, Lower Is Better

***High Performance Analog Solutions from Linear Technology***

As design techniques and process technologies improve, many IC products focus on the big numbers – more bandwidth, more resolution, more output power, more throughput, more FLOPS. The list goes on. But for precision op amps, the critical factors get smaller as they get better – low supply current, low voltage operation, low offset voltage, low noise, low input bias current, etc. These are the factors that small signal designers concern themselves with the most. The latest amplifiers use innovative designs and processes that deliver performance that continues to exceed users' expectations.

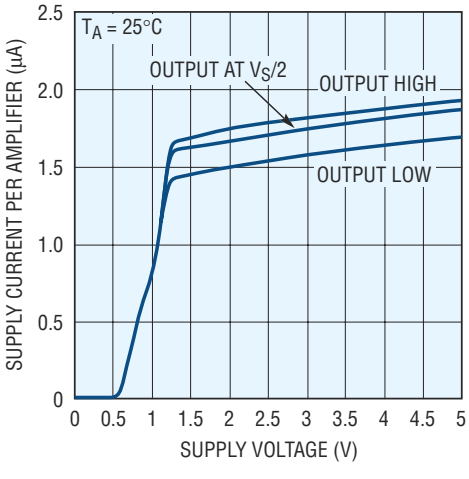


**Figure 1. LT6003 family behaves well during power up sequences under the most stressful conditions.**

## Low Supply Current and Low Voltage Operation

For applications requiring operation from two AA batteries, size and power consumption are obvious and primary concerns. If precision performance is also required, there is no choice better than the LT6003 (single), LT6004 (dual), and LT6005 (quad) micropower op amps from Linear Technology. This family of amplifiers operates from 1.6V with only 1µA max supply current at 25°C and 1.6µA max over the full industrial temperature range of –40°C to +85°C. The LT6003 single op amp is available in a tiny 2mm x 2mm DFN package and offers 500µV maximum offset and excellent drift performance at 2µV/°C. As important as these specifications are, designers need to look beyond the spec table to see one of the most important benefits of this amplifier.

For many micropower amplifiers, the guaranteed micropower operation applies only in limited operating conditions. Rail-to-rail operation, for example, compromises the supply current, with up to a threefold current increase as the output approaches the rails. When operating on as little as 1.6V, rail to rail operation is critical to maximize dynamic range and it is important for the amplifier to maintain micropower operation in these cases. As an amplifier powers up, its outputs and inputs are consequently near the supply rails. If designers do not consider this unspecified behavior, many micropower amplifiers may demand current that exceeds the capability of the power supply, preventing a successful power-up sequence. The LT6003 family employs special design techniques to behave gracefully over the entire operating range for true micropower operation. Figure 1 shows the behavior of the LT6003 under the most stressful power up conditions for a micropower op amp.

## CMOS Op Amps Offer Low Bias Current

For digital designers, CMOS process technologies have long offered superior performance to older bipolar processes. Substantial benefits of higher speed, lower power consumption, and lower cost have relegated bipolar digital devices to the realm of ancient history. In the world between on and off, analog IC designers have a much different view of bipolar process technologies. Most high performance op amps still use bipolar processes that offer a lot of benefits in analog designs with only a few drawbacks.

The one factor that keeps precision CMOS amplifiers viable is input

# For These Amplifiers, Lower Is Better

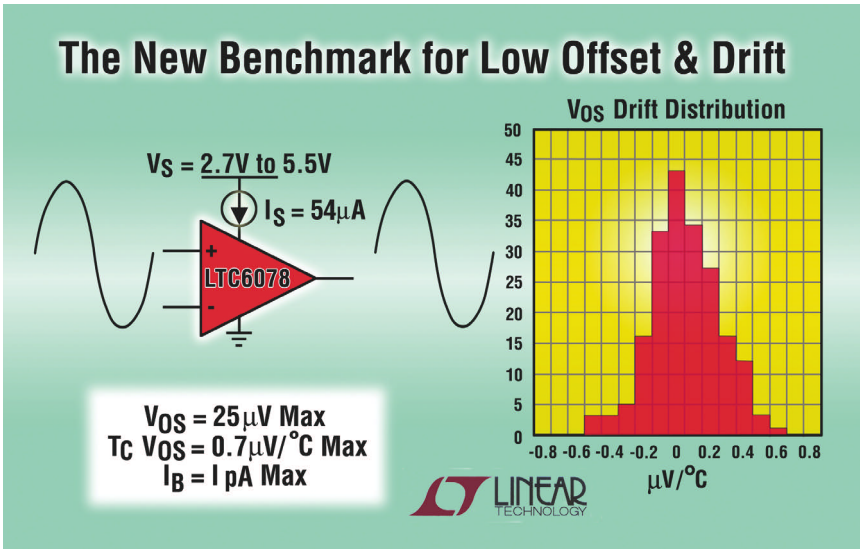


**Figure 2. LTC6078 Low Offset, Low Drift CMOS Op Amp**

low bias current ($I_B$). Bipolar transistors are current controlled devices, so bias current is inevitable in a bipolar op amp. Because MOS transistors are voltage controlled, there is virtually no $I_B$ in a CMOS op amp. In fact, the $I_B$ specification of an op amp is more likely to be due to leakage of input protection diodes than the gate current of the input transistors themselves. In applications with high impedance signal sources, $I_B$ can be the largest single source of error in the signal chain.

CMOS has its disadvantages as well. Noise and device matching limitations plague this process technology. However innovative new design and process techniques from Linear Technology combine the advantages of low offset and low noise of bipolar amplifiers with the low input bias current of CMOS inputs. Two amplifier families emerge that address these shortcomings, enabling power reduction and performance improvements in low-power and telecommunications applications.

## Low Offset and Low Input Bias Current

For many precision applications requiring low offset voltage ($V_{OS}$) and drift performance, CMOS chopper-stabilized amplifiers have often been the solution of choice. By using switching techniques to synchronously cancel the inherent DC imbalances of the amplifier, the $V_{OS}$ and drift can be very close to zero. The price for this performance has been high power consumption and noise at high frequencies due to the clocking circuits.

The LTC6078 (dual) and LTC6079 (quad) employ innovative trimming circuits that yield $V_{OS}$ of only 25µV maximum with $V_{OS}$ drift of 0.7µV/°C as shown in Figure 2. This $V_{OS}$ performance is as good as some chopper-stabilized amplifiers and the best bipolar amplifiers while offering 1pA max input bias current at 25°C that a CMOS amplifier can deliver. Combining these outstanding input specifications with maximum supply current of 54µA per amplifier and 2.7V operation, the LTC6078 and LTC6079 extend the capabilities of power-sensitive systems.

Current sensing in handheld, battery-operated devices can be improved significantly with the benefits offered by the LTC6078 op amp. The circuit in Figure 3 shows a standard op amp current sense circuit. The power dissipated by the sense resistor entices designers to use the lowest possible value. The impact of op amp errors increases as the value of the sense resistor, $R_S$, decreases. If the op amp in Figure 3 had a $V_{OS}$ of 1mV, the measurement error would be 0.1% with a 1Ω resistor. Because of the 25µV max $V_{OS}$ of the LTC6078, the designer can reduce sense resistor power dissipation by a factor of 40 by using a 25mΩ sense resistor and maintain the same system precision.

## Low Noise and Low Bias Current

CMOS transistors inherently generate more low frequency (1/f) noise

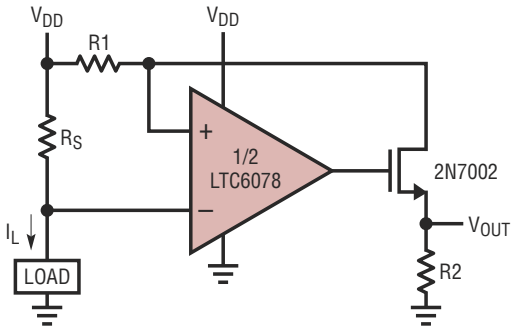


**Figure 3. The precision of the LTC6078 enables a small Rs value reducing power dissipation without sacrificing DC accuracy.**

than comparably sized bipolar transistors. The 1/f noise corner can be orders of magnitude lower in bipolar amplifiers. Consequently, bipolar amplifiers are the traditional choice for low noise applications. However, some low noise applications also require the low input bias current offered only by a CMOS amplifier.

Increased transistor area is required to reduce the fundamentally higher 1/f noise of CMOS transistors. But the increase in area also increases gate capacitance, which increases the input capacitance of a CMOS op amp. If the input capacitance is non-zero, the high frequency input impedence is far from ideal. The noise gain of an op amp is governed by $V_{OUT}=V_{NOISE}*(1+Z_F/Z_I)$, where $Z_I$ includes the input impedance of the amplifier as well as the discrete input resistor. An amplifier with large input resistors may have low noise, but high input capacitance creates high noise gain. This only trades a 1/f noise reduction for an increase in wide band noise content at the output.

The LTC6240 (single), LTC6241 (dual) and LTC6242 (quad) have very large input devices to reduce the 1/f noise to only 550nVp-p, a figure that rivals a good, low-noise bipolar amplifier. Though one would expect large input capacitance from such large input structures, the LTC6240 family utilizes an innovative capacitance cancellation technique resulting in a total input capacitance of 3.5pF, a third of competitive CMOS op amps. Figure 4 compares the benefits of this design technique with other low noise CMOS op amps that do not employ capacitance-canceling circuits. The great combination of performance of the LTC6241 with noise comparable to good bipolar amplifiers and 1pA bias current substantially improves the performance of low noise, photodiode amplifiers and high impedance sensor applications.

## The Ideal Op Amp

Op amps are useful because their rules are simple and few. The basic non-inverting gain equation $V_{OUT}=V_{IN}*(1+R_F/R_I)$, for example, is about as simple a guiding rule as one will find in the analog realm. This equation, however, is simple only because it makes certain assumptions including:

- infinite input impedance
- zero input current
- zero offset voltage
- zero noise voltage
- zero noise current

In some applications, errors due to these unrealizable assumptions are inconsequential. However, as the industrial world requires increasingly higher precision, there are many applications that require amplifiers to push these limits closer and closer to the ideal.

For example, high impedance sensors and photodiode amplifiers are very sensitive to noise and input bias currents. Low power current sense circuits benefit from ultra-low offset voltage and rail-to-rail operation.

Although by definition unachievable, the ideal op amp offers a complete collection of specifications to offer as targets for analog designers. Every application requires a different combination of specifications and the number of op amps continues to expand to fit those needs.

# For These Amplifiers, Lower Is Better

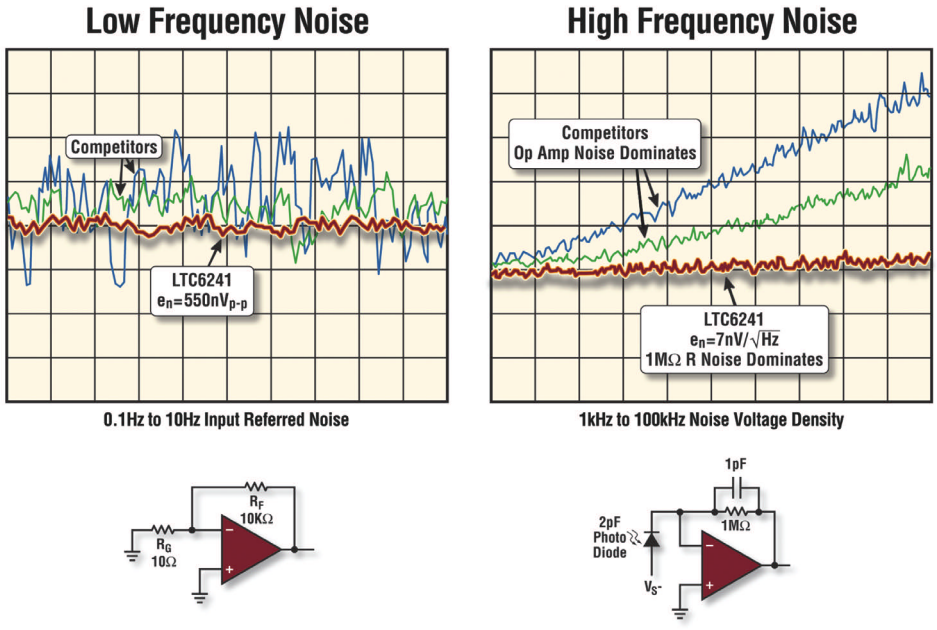


**Figure 4. Input Capacitance Cancellation techniques enable the CMOS LTC6241 to offer outstanding low frequency noise performance and maintain low noise gain.**

The low noise CMOS amplifier family from Linear Technology extends to high frequency applications with the introduction of the LTC6244. This 50MHz amplifier maintains 5.6pF total input capacitance for low noise gain and offers outstanding DC input performance. This combination of performance is important in many wideband sensor conditioning applications. High impedance sensors such as SONAR receivers, and LVDTs require low input bias current and low noise. The lower –3dB bandwidth of the AC difference amplifier shown in Figure 5 is set by R5 and C3 with the upper bandwidth set by R2 and C1. The DC output voltage is $V_{REF}$ regardless of the DC common mode voltage. With the values shown, the gain is 10 and the total input referred wideband noise is 4.5µVrms from 500Hz to 200kHz.

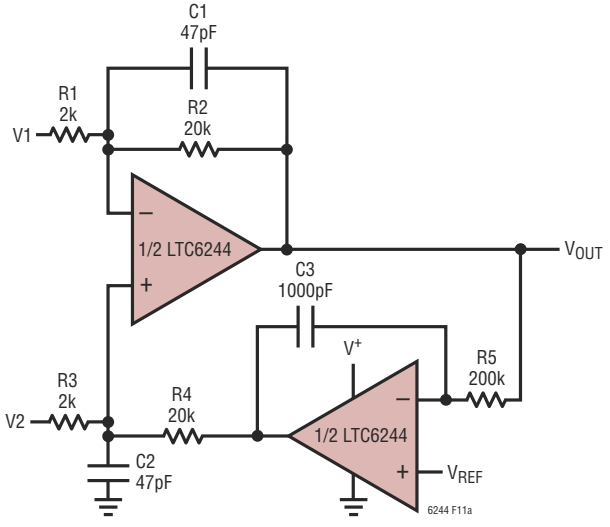


**Figure 5. An 800Hz to 160kHz Low Noise AC Difference Amplifier with a Gain of 10.**

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# Downlink enables remote boundary-scan tests

LINK INTERNAL IEEE 1149 STRUCTURES WITH COMMUNICATION PORTS INTEGRATED WITHIN A PRODUCT AND AVAILABLE TO THE OUTSIDE WORLD.

For some time, engineers have followed the IEEE 1149.1 standard, also known as "boundary-scan," to create test structures on pc boards and in complete systems. Unfortunately, once products leave a production line, engineers may lose physical access to their five-pin IEEE 1149 connectors or to the five test points that a bed-of-nails tester uses. So, although equipment may still include IEEE 1149 test capabilities, engineers cannot access them.

To skirt this problem, you can link internal IEEE 1149 structures with communication ports integrated within a product and available to the outside world. As a result, engineers can use a USB port, an Ethernet port, a wireless telemetry channel, or another medium to transfer test information to and from IEEE 1149-capable equipment, such as a satellite or remote embedded systems, but without physical access to the test, or boundary-scan, signals. (Engineers often refer to the technology that underlies IEEE 1149 as "boundary scan" or "JTAG." JTAG stands for the Joint Test Action Group that developed the IEEE standard.)

This technique requires minor design modifications that add a downlink module to the system you wish to test—the DUT (device under test). But, the renewed access to test capabilities from a distant location justifies the small added cost. Implementation also requires an uplink module near the boundary-scan-test controller—typically, a PC (**Figure 1**). The remote-communication technique also lets you test several distant systems in parallel (**Figure 2**) for a 4-to-1 boundary-scan TAP (test-access port).

The communication modules convert to and from a protocol, such as TCP/IP (Transfer Control Protocol/Internet Protocol), and the standard five-wire IEEE 1149 signals that would otherwise electrically link a tester to a target system. The five-wire boundary-scan controller connects directly to the uplink module. And the downlink module provides the five-wire connections to the boundary-scan devices in the target system. In effect, the modules and the communication link operate transparently to the controller and target.

## KEEP TEST SOFTWARE

The communication links and hardware modifications to the target system require no changes to test software. An added utility program establishes communications and calibrates any send-receive latency due to cable length or network delays. This approach yields high testing speeds over long distances for a communication medium such as 10-Gbps Ethernet.

Although it seems counterintuitive, a communication protocol such as Ethernet TCP/IP provides advantages over

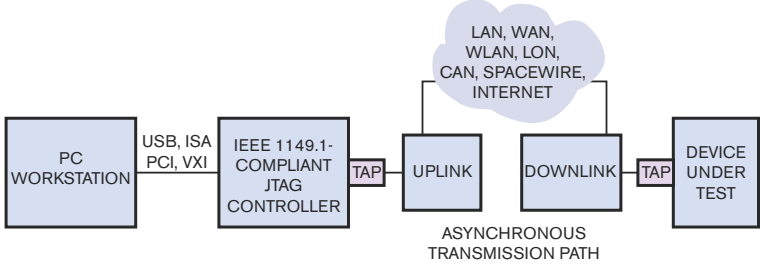


Figure 1 Remote IEEE 1149.1 testing involves placing uplink and downlink modules and an asynchronous communication path, such as an Ethernet network, between the test controller and the device under test.

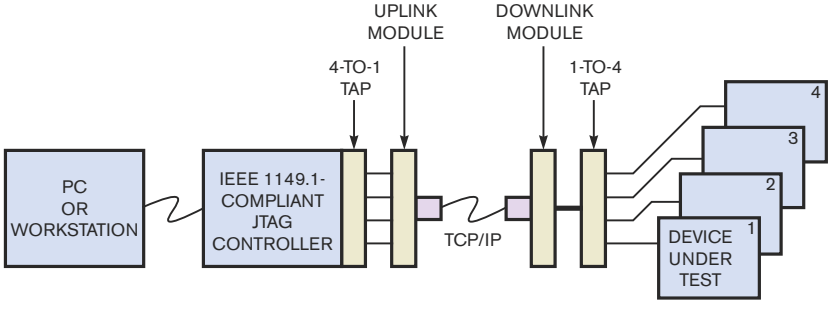


Figure 2 Remote testing also can accommodate parallel testing of several devices. In this case, a 4-to-1 test-access-port circuit multiplexes the test and result vectors.

direct boundary-scan connections. First, the TCP/IP includes error detection, a capability that the IEEE 1149.1 standard does not define. Thus, should a communication error occur, the receiver can request a retransmission.

Second, encryption/decryption software for TCP/IP communications can help protect intellectual property embedded in a design or implied within boundary-scan information. Likewise, encryption protects "bit streams" transmitted through a boundary-scan channel to configure FPGAs.

Implementing the downlink functions in hardware, perhaps in an inexpensive PLD (programmable-logic device), eliminates the need for a separate IEEE 1149.1-compliant test controller within the target system. And, because the communication medium appears transparent to the controller and the DUT, engineers can continue to use the same boundary-scan-test vectors.

A typical network topology shows communications and test applications in a manufacturing facility (**Figure 3**). This remote-test configuration provides protocol converters at the uplink and the downlink modules. The downlink module may exist as part of the target system or external to it.

Boundary-scan operations occur in a synchronous process (**Figure 4a**). The test controller and the DUT sample all inputs on the rising edge of the TCK (test-clock) signal. These inputs comprise TDI (test-data input) and TMS (test-mode select) at the DUT and TDO (test-data output) at the test controller.

Likewise, the controller and DUT update all outputs on the falling edge of the TCK signal. These outputs comprise TDO for the DUT and TDI and TMS for the tester. The falling edge of TCK also causes the DUT to shift out its TDO signal. On the next rising edge of TCK, the boundary-scan controller samples the TDO signal to obtain test results, one bit at a time.

Remote boundary-scan operation requires the transmission of only the TMS and TDI bits from the controller to the target during each TCK cycle. The downlink module generates a local clock upon receipt of TDI and TMS information. So, the uplink does not transmit clock information to the target. The local clock in the downlink module operates only during testing and not during normal operation of the DUT.

This approach assumes the use of error detection and correction. Upon reception of a valid packet, the downlink circuit reproduces the TDI, TMS, and TCK signals and applies them to the target's boundary-scan chain. In return, the downlink transmits the valid TDO signal to the uplink,

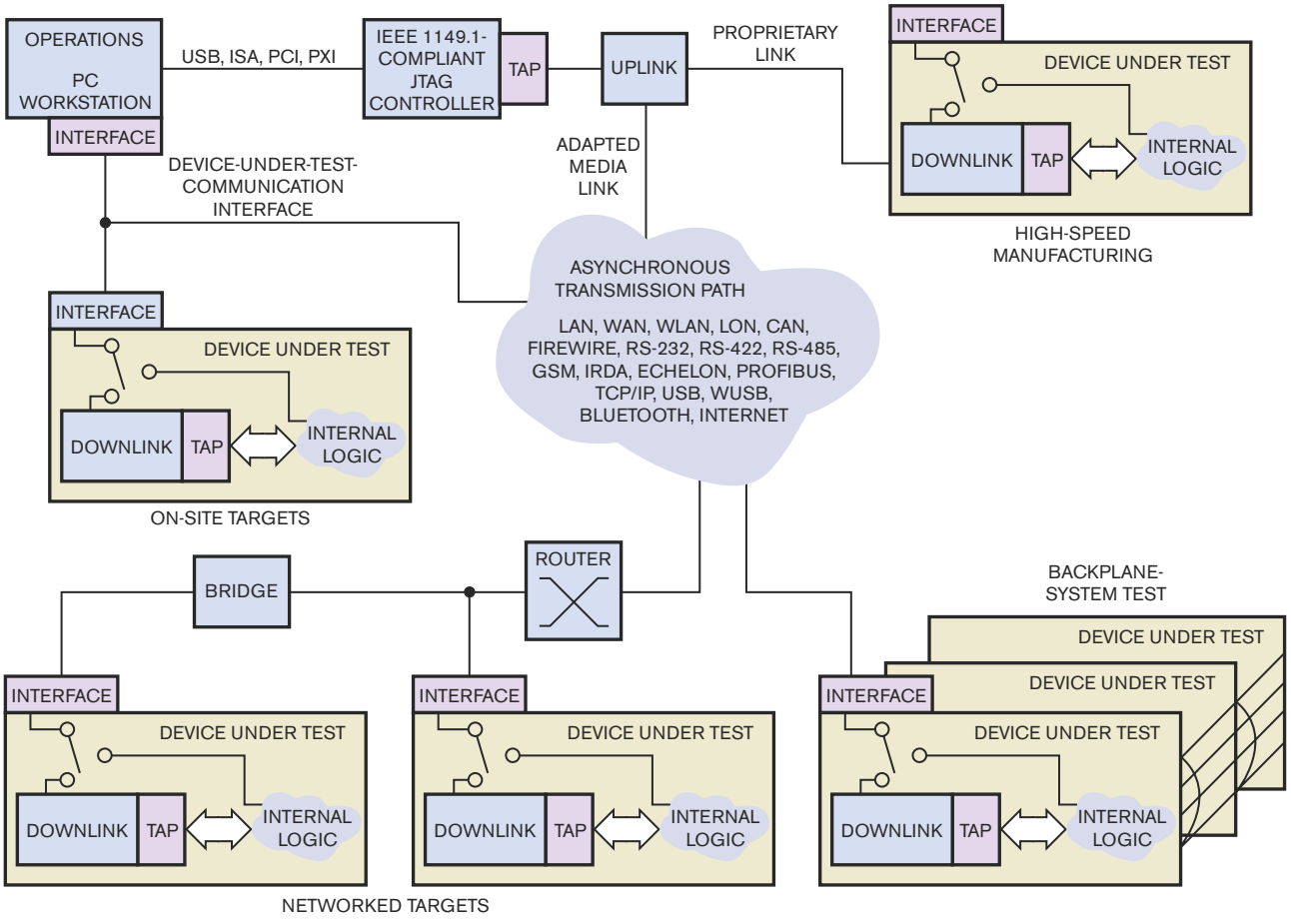


Figure 3 A large network that performs remote boundary-scan tests can accommodate a variety of transmission paths and devices or boards to test.

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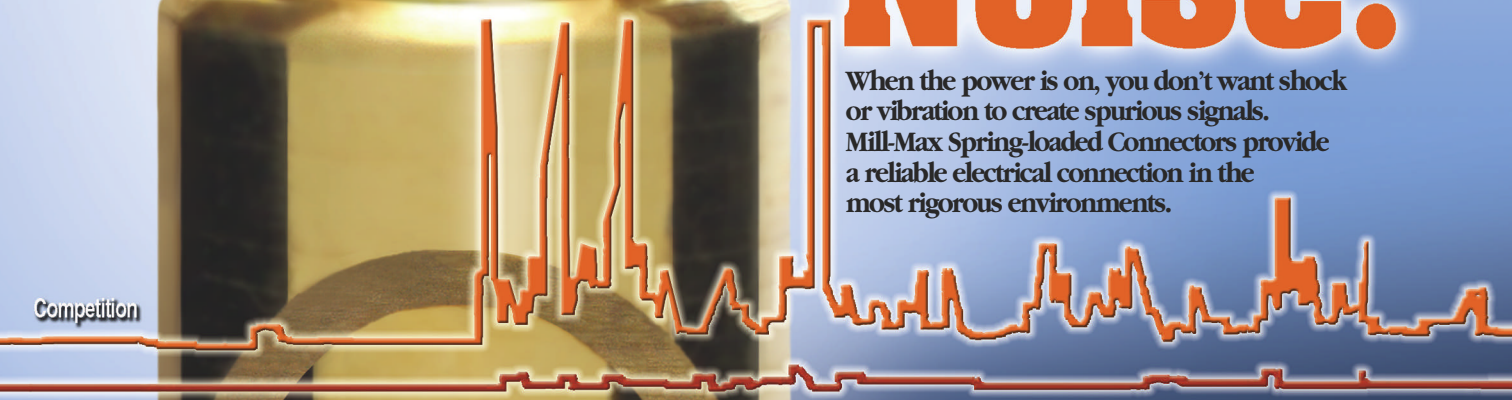


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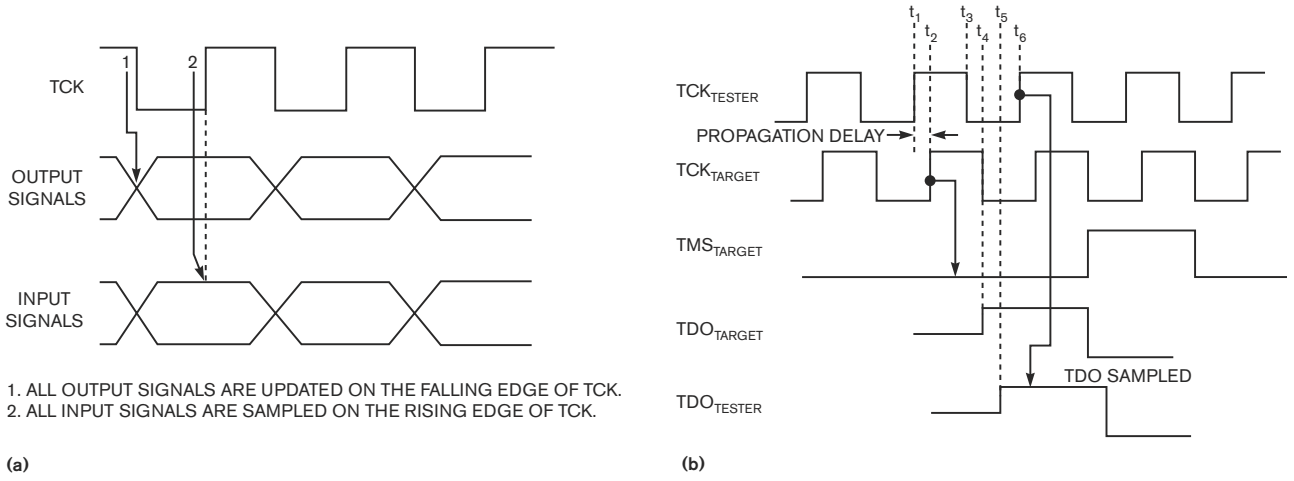


Figure 4 Synchronous IEEE 1149.1 test signals illustrate normal timing relationships. All output signals are updated on the falling edge of TCK, and all input signals are sampled on the rising edge of TCK (a). A transmission path between a test controller and the DUT introduces a delay, skewing the test signals (b).

which decodes the communication packet and synchronizes the received TDO signal at the test controller for comparison with the expected TDO data.

## ACCOUNT FOR PROPAGATION DELAY

Boundary-scan operations conducted remotely vary in timing from those that occur with a direct five-wire connection. To explain the remote-test timing, it helps to first review the effect of propagation delays on a direct connection.

The synchronous operation of a boundary-scan controller limits the length of the cable that connects the controller to a target DUT. An allowable cable length relates directly to the frequency of the TCK signal (**Figure 4b**). Note the delay between the $TCK_{TESTER}$ ($t_1$) and the $TCK_{TARGET}$ ($t_2$) signals

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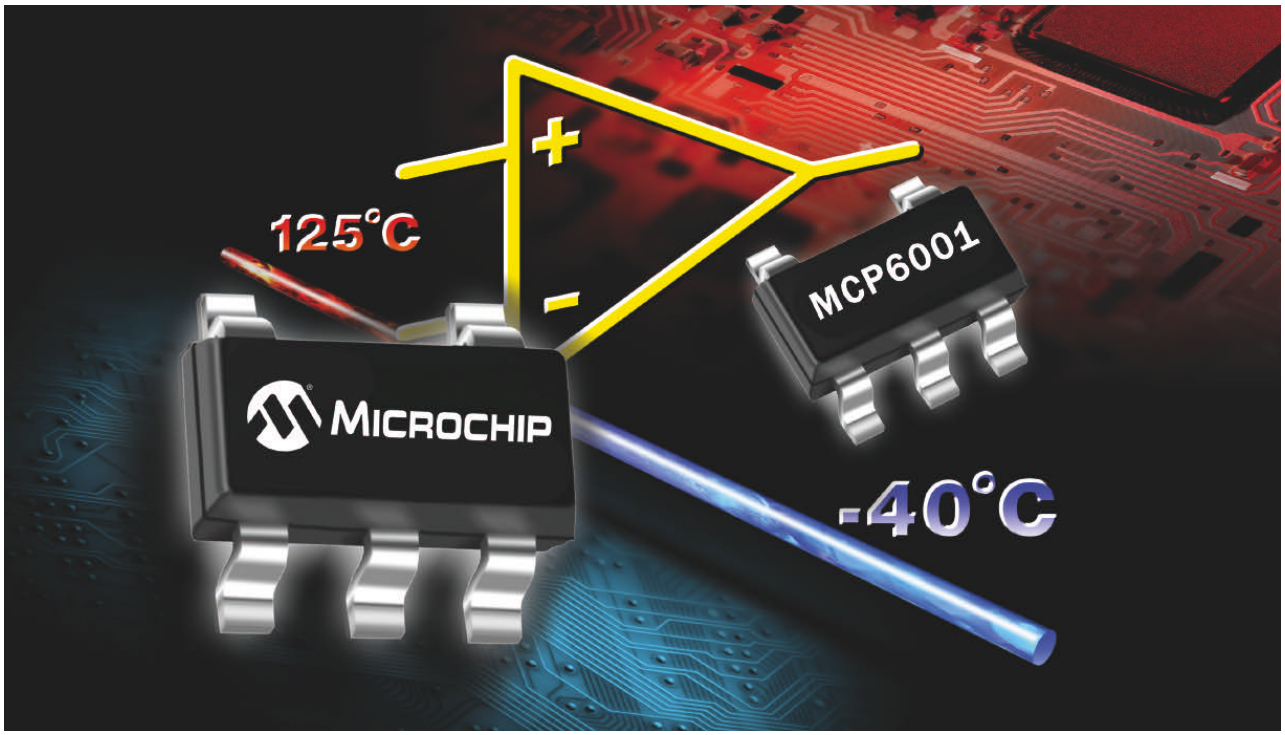


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| MCP6241/2/4 | 550 kHz | 50 | 5.0 | 45 | 1.8 – 5.5 |
| MCP6001/2/4 | 1 MHz | 140 | 4.5 | 28 | 1.8 – 5.5 |
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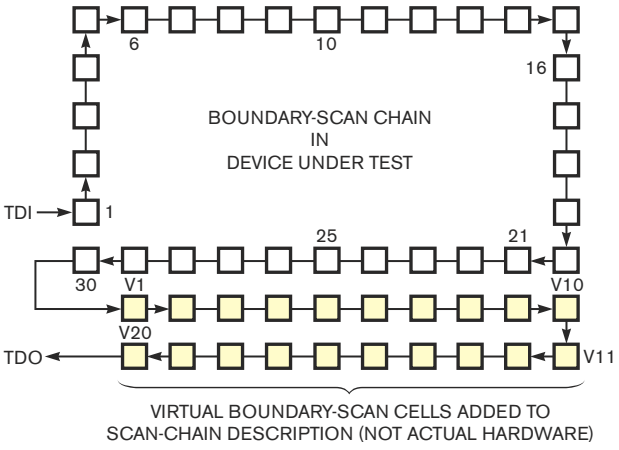


Figure 5 Adding virtual cells to the description of the boundary-scan chain causes the test controller to "delay" processing the TDO signal by an amount equal to the communication link's propagation delay. These cells do not exist in hardware.

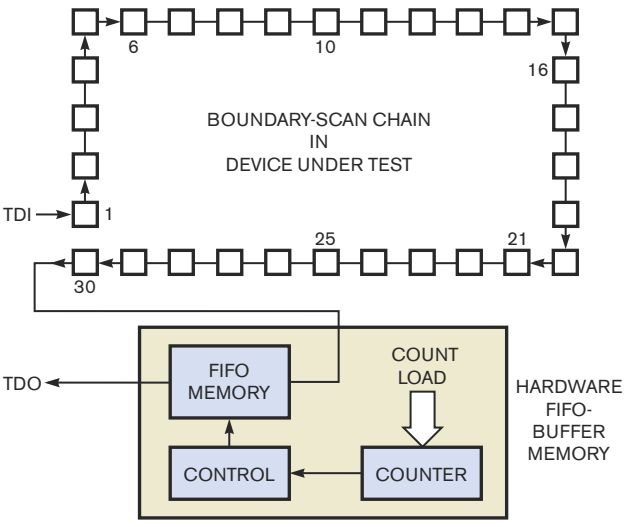


Figure 6 Implementation of a FIFO memory compensates for the actual delay. The virtual-cell counter decrements a value that corresponds to the delay measured in TCK cycles. When the count reaches zero, TDO data shifts into the test controller.

due to propagation delay in a cable. On the rising edge of $TCK_{TARGET}$ ($t_2$), the target samples the TMS and TDI lines. On the falling edge of $TCK_{TARGET}$ ($t_4$), the target updates its TDO output and places it on the cable. Due to the delay in the cable, the new TDO information reaches the controller at $t_5$. The test controller samples the new TDO information on the rising edge of $TCK_{TESTER}$ ($t_6$). Thus, the time available for the TDO signal to travel from the last boundary-scan output on the target to the test controller amounts to half the TCK period.

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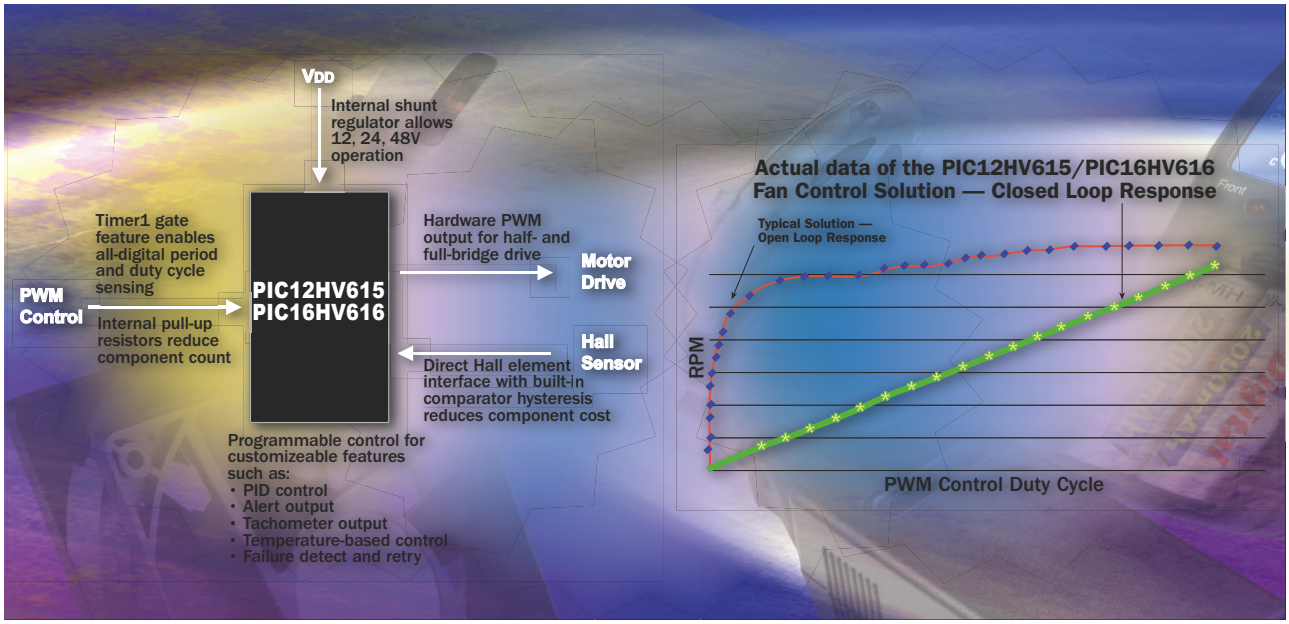


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| PIC16HV616 | Yes | 3.5 KB/2 Kw | 8 | 2 | Full bridge | 8 MHz |

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Assume a 10-MHz TCK frequency, or a 100-nsec period. In this case, the TDO data must travel from the last DUT in the chain to the test controller in 50 nsec or less. If you assume a cable propagation delay of 5 nsec/m, you must use a 10m or shorter cable.

Now, assume that you have a remote target system and that you cannot control the delay. If a network connection causes a 100-msec delay, you could use a maximum TCK frequency of only 5 Hz (1/100 msec×½=5 Hz), which would cause extremely long tests. Thus, a system that relies on long cables or experiences network delays must provide a means of overcoming the delay without greatly reducing test times.

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## VIRTUAL CELLS SYNCHRONIZE TDO DATA

To let the TCK frequency run at a reasonable rate—which depends on the communication channel's bandwidth—and to account for the communication delay, you can "add" virtual cells to the end of the TDO chain in the target system. These cells *do not exist*. You simply adjust the test software to include these nonexistent cells in the scan chain. As a result, the test software delays accepting the target system's TDO data for the time it would take the TDO data to shift through these additional cells (**Figure 5**). Utility software measures propagation delay and communication-link speed to determine the number of cells to add to the target system's scan chain.

Consider a system in which the TDO data bits received from the downlink module have a delay of 1 to 2 sec, and the tester's TCK output produces a 4-MHz clock signal. In this case, the uplink module must provide a buffer memory to store all TDO information it received before the tester expects to receive it. The buffer could require 4 to 8 Mbits of storage, which DDR-memory devices could provide.

In the uplink module, a FIFO memory buffers the TDO data and compensates for the measured delay (**Figure 6**). As soon as the uplink module starts to send relevant TDI information to the downlink module, it loads the virtual-cell counter with a value that corresponds to the communication delay as expressed in TCK cycles.

Simultaneously, the uplink module temporarily stores in the FIFO memory the TDO bits it receives from the downlink module. Each TCK cycle decrements the virtual-cell counter until it reaches zero. At that time, the controller starts to continuously shift out the accumulated TDO bits at the TCK rate. Thus, the combination of the added virtual cells in the TDO chain and the FIFO properly synchronize the TDO bits with the test controller's TDO input.

One objective is to efficiently transmit test data for multitap test applications within a single data packet. During the

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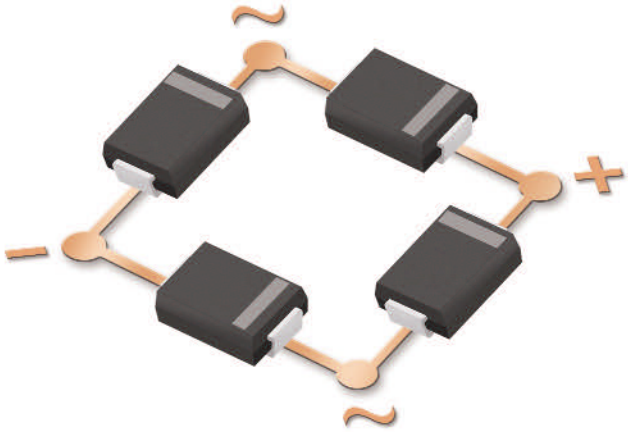

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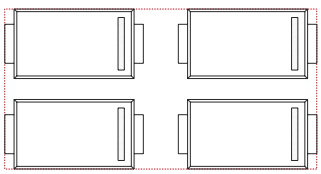

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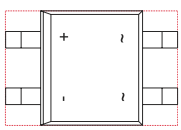

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uplink-encoding process, you store test information as a 16-bit block for every TCK cycle. This 16-bit block contains the boundary-scan information—TDI, TMS, and optional signals—for a maximum of four individual boundary-scan chains. To efficiently use the communication channel's bandwidth, the downlink module encodes four TDO bits for each of the four chains into a 16-bit block.

To ensure that the downlink module transmits only relevant TDO data, the module includes a state machine that determines when the target TAPs are in the shift state. Similarly, the uplink module provides a state machine that synchronizes events that occur at the target system.

In this way, the uplink can recognize valid TDO data and transmit only the valid bits to the test controller for comparison. As a result, the uplink module can compensate for the round-trip transmission delay of potentially many TCK periods with the inclusion of a "virtual component" (**figures 5** and **6**).

## MEASURING LATENCY

A software utility establishes the communication channel between the uplink and the downlink modules, and it performs a loop-back test to measure the latency in the channel. Based on a latency calculation, the utility configures the proper number of virtual cells to add to the boundary-scan chain the test software will "see." The software may add some overhead in the calculation to ensure that, once the virtual-cell counter reaches zero, the FIFO memory provides valid TDO data. In a point-to-point channel with a known latency, the software utility can simply establish the uplink-to-downlink connection and configure a preset number of virtual cells.

This approach to remote boundary-scan testing has limits, due to the need to partition test-bit patterns into separate data packets, the size of which depends on the protocol you choose. These packets can contain a high proportion of overhead information, which decreases the bit efficiency of transmissions.

In addition, the process requires a downlink controller that extracts TDI and TMS information from each packet and distributes these signals throughout the target system. The downlink also must temporarily store the resulting TDO data before transmission to the uplink at the test controller. EDN

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## AUTHOR'S BIOGRAPHIES


*Marc van Houcke is a design engineer at JTAG Technologies. He holds a bachelor's degree in digital electronics. For the last nine years, he has worked in design and development of boundary-scan controllers and related tools. He has also provided application and design-for-test support and has trained other engineers.*

*Anthony Sparks has more than 12 years of experience in test engineering, and he has focused on in-circuit and boundary-scan test. He currently works as a technical-marketing consultant at JTAG Technologies. His duties include participating in IEEE Standards Working Groups, assisting customers with system-level and advanced boundary-scan implementations, and developing strategic partnerships.*


## ACKNOWLEDGMENT


*Thanks go to Ilkka Reis of Patria Advanced Solutions and Mikko Simonen with Nokia Mobile Phones in Finland, who developed the patented TapSpacer technology.*

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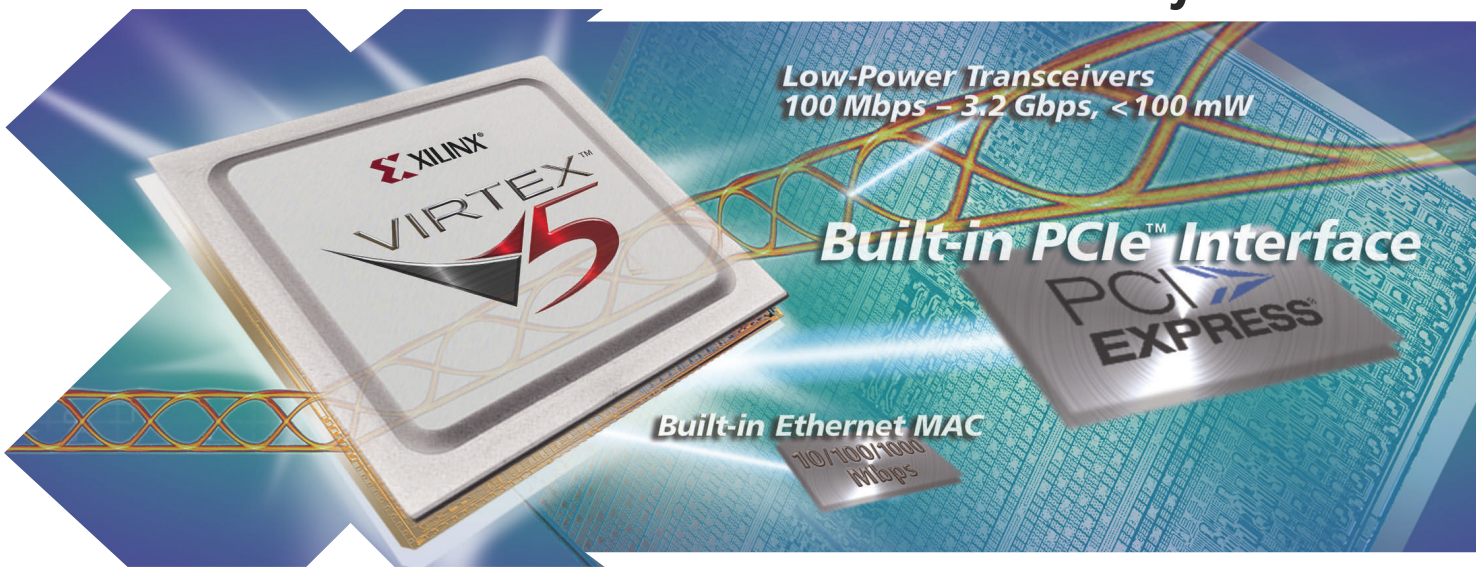


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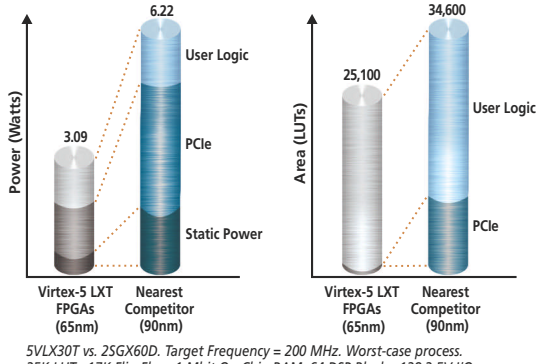


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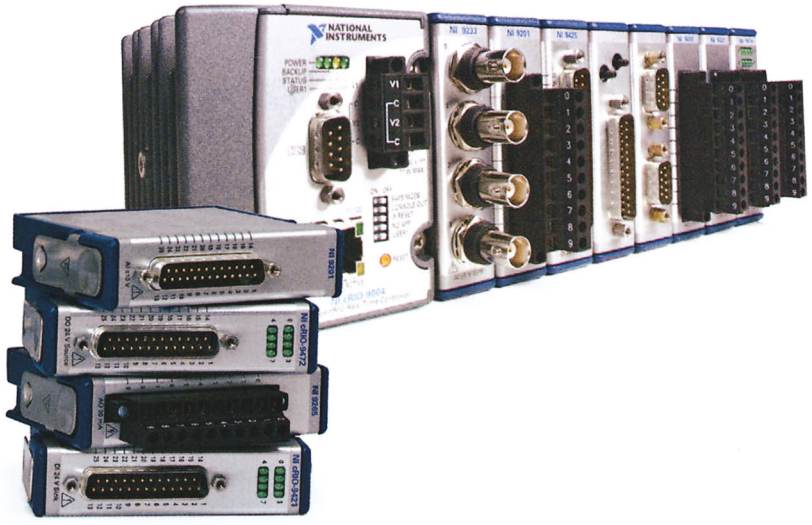



| Applications | Vehicles |
|---|---|
| • Data logging | • Automotive |
| • Durability testing | • Military |
| • Vehicle dynamic testing | • Aerospace |
| • Brake and suspension system testing | • Railroad |
| • Crash testing | • Agricultural |
| • Noise, vibration, and harshness (NVH) | • Recreational |
| • ECU rapid control prototyping | • Mining/construction |
| • Hardware-in-the-loop (HIL) test | • Marine |

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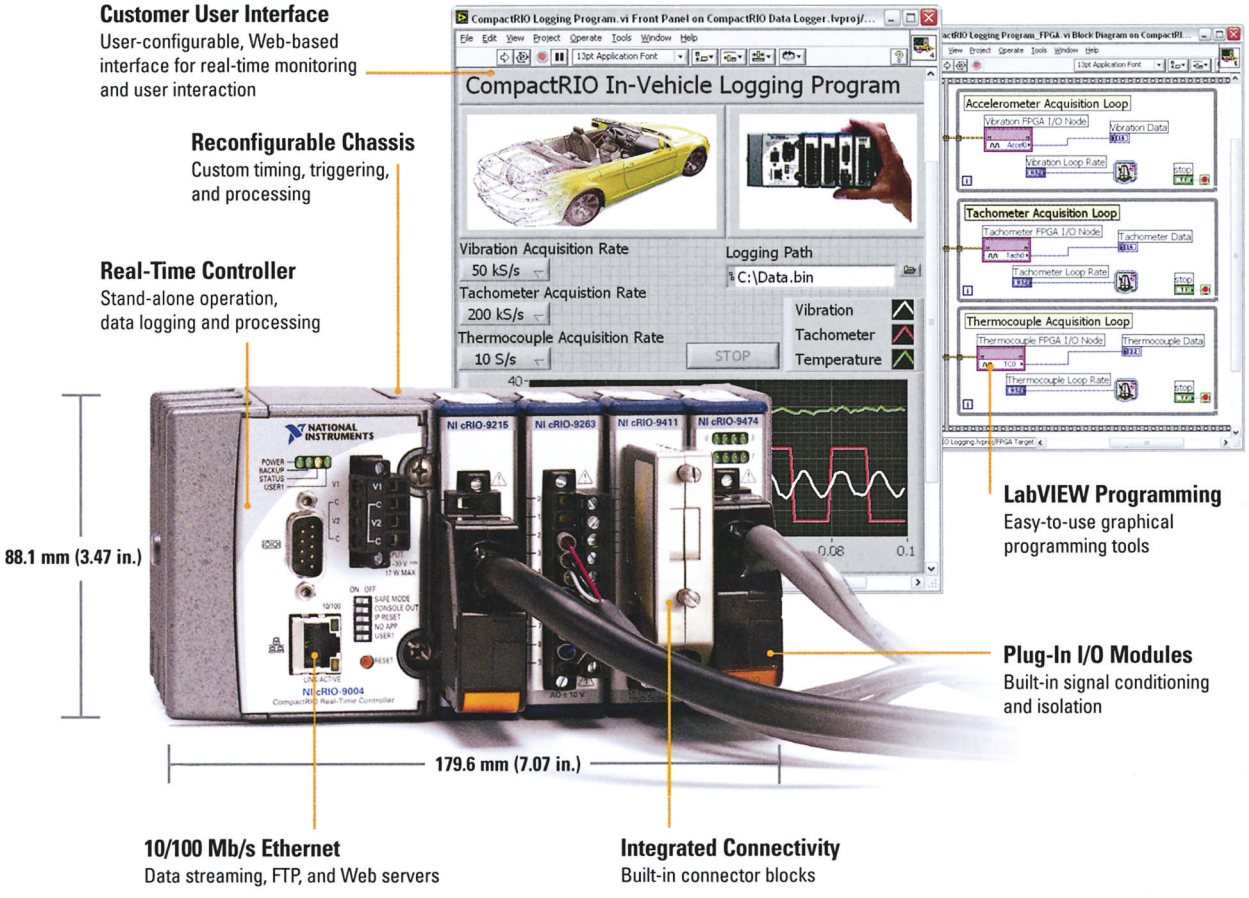
To learn more about CompactRIO, visit **ni.com/compactrio**.

## Rugged Platform

The mechanical design of CompactRIO creates a system that can withstand the rigors of any in-vehicle testing environment. CompactRIO is rated for -40 to 70 °C operating temperature range, 50 g of shock, and up to 2,300 $V_{rms}$ isolation (withstand) and maintains international safety, electromechanical compliance (EMC), and environmental certifications.




## Powered by LabVIEW

With CompactRIO, you can create a custom and intelligent in-vehicle data-logging and analysis system using LabVIEW graphical programming tools. Quickly program and configure CompactRIO for any in-vehicle application in five steps:

**1: Develop** LabVIEW program on your PC

**2: Download** the program to CompactRIO

**3: Deploy** CompactRIO to vehicle to acquire and log data

**4: Transfer** data from CompactRIO to your PC

**5: Analyze** data with NI LabVIEW and DIAdem

## Most Popular CompactRIO In-Vehicle I/O Modules

| I/O | Sensor and Signal Type | Module | Channels | Special Features |
|---|---|---|---|---|
| Temperature | Thermocouple | NI 9211 | 4 | 24-bit delta-sigma, 15 S/s, differential (J, K, R, S, T, N, E, and B thermocouple types) |
| Sound and Vibration | IEPE Sensors (Accelerometer/Microphone) | NI 9233 | 4 | 24-bit, 50 kS/s, simultaneous, IEPE conditioning, built-in antialiasing |
| Strain and Load | Bridge-Based Sensors (Strain Gages and Load Cells) | NI 9237 | 4 | 24-bit, 50 kS/s, simultaneous, full/half/quarter-bridge support, antialiasing |
| Voltage | ±200 mV to ±10 V | NI 9205 | 32 | 16-bit; ±200 mV; ±1 V, ±5 V, and ±10 V programmable ranges; 250 kS/s; 32 single-ended |
| | ±60 V | NI 9221 | 8 | 12-bit, 800 kS/s, single-ended, isolation |
| Fuel Cell | ±200 mV to ±10 V | NI 9206 | 16 | 16-bit; ±200 mV; ±1 V, ±5 V, and ±10 V programmable ranges; 250 kS/s; 16 differential channels; 600 VDC (U.S.)/400 VDC (EU) CAT I bank isolation |
| Digital I/O | 5V/TTL | NI 9401 | 8 | 100 ns, 5 V TTL, high-speed digital I/O, bidirectional, isolation, 30 V protection |
| Memory Storage | Secure Digital (SD) Storage | NI 9802 | 2 | 2 slots for SD cards, up to 4 GB per module, 2 MB/s logging rates |
| CAN Communication | 2-Port, High-Speed CAN | NI 9853 | 2 | Transmit/receive 100% bus load at up to 1 Mb/s, ISO 11898 compliant, 11 and 29-bit arbitration, standard DB-9 male connector for each port |

**For a complete list of more than 30 CompactRIO I/O modules, visit ni.com/compactrio.**

### Connectivity to Any Sensor Type

CompactRIO provides more than 30 I/O modules for connecting to any in-vehicle sensor, actuator, and network. CompactRIO modules contain built-in signal conditioning for sensors such as thermocouples, RTDs, strain gages, accelerometers, and microphones as well as isolation.

### I/O Timing and Synchronization

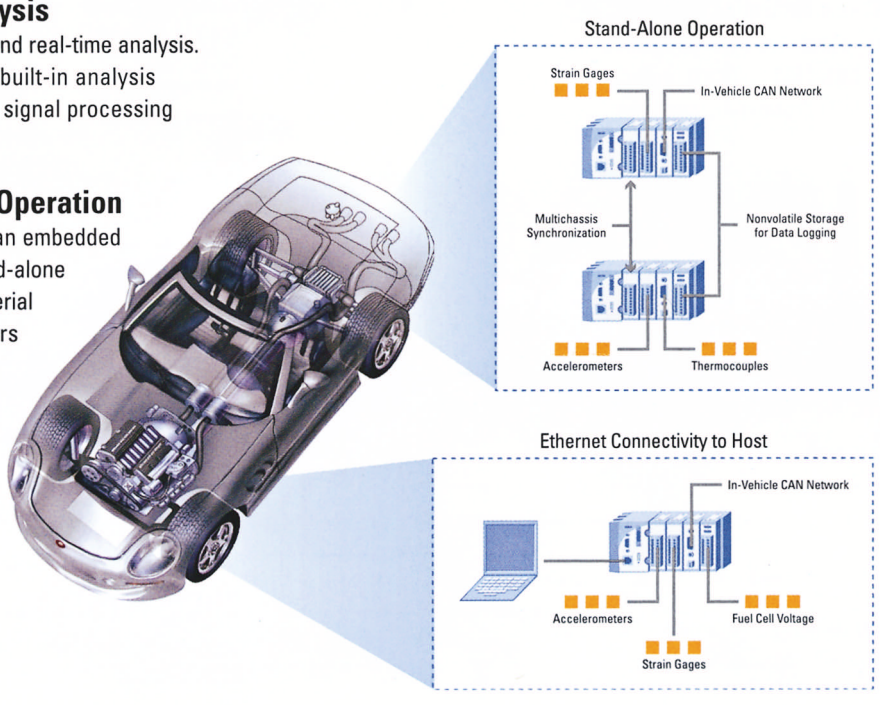
With CompactRIO, you can customize the sampling rates on a per-module basis. CompactRIO can acquire temperature measurements at 10 S/s while monitoring vibration measurements at 50 kS/s. You can also synchronize all I/O within a CompactRIO system with nanosecond resolution.

### Signal Processing and Analysis

CompactRIO can perform processing and real-time analysis. NI LabVIEW contains more than 600 built-in analysis functions to perform advanced digital signal processing on any sensor signal.

### Stand-Alone or Networked Operation

The CompactRIO controller contains an embedded real-time processor for intelligent stand-alone operation and includes Ethernet and serial ports for connection to host computers and peripherals. With dual 9 to 35 V (6 to 35 V during operation) power supply inputs, you can power CompactRIO directly from a vehicle battery.

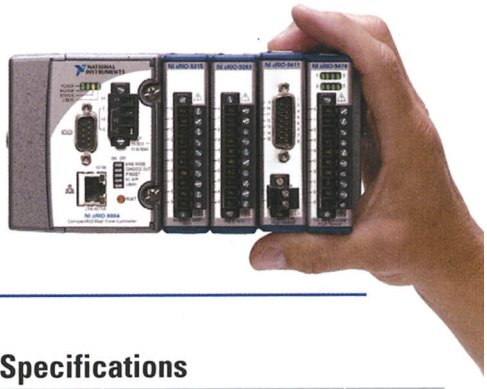



**"The advantage of National Instruments CompactRIO is its small size and flexibility. With CompactRIO, we created a portable, user-defined onboard vehicle analysis and diagnostics system."**

***Rainer Lindner, Hardware Engineer at GÖPEL electronic***

**"The small size and ruggedness of the CompactRIO platform made it the ideal solution for an in-vehicle test system that could survive in the harsh environment of our test course."**

***Andrew Leslie, Systems Engineer at PACCAR***



## High-Speed Control

For control applications such as rapid control prototyping, CompactRIO permits closed-loop control at extremely fast rates. Using any of the I/O modules, you can program CompactRIO to respond to incoming CAN, analog, or digital data and make decisions at rates up to 40 MHz.

## Build Custom In-Vehicle I/O Modules

You also can develop custom modules to meet specific in-vehicle I/O needs. Third-party companies have built the following modules for CompactRIO:

- GPS monitoring and synchronization module
- GPRS wireless communication module
- GSM wireless data exchange module
- Local Interconnect Network (LIN) communication module
- ARINC-429 avionic protocol module
- MIL-1553 mil/aero protocol module
- ECU prototyping modules

*This custom module from S.E.A. includes both wireless GSM and GPS functionality.*

Visit **ni.com/compactrio** to download FREE application notes and example programs for:

- In-vehicle data logging
- NVH measurements and analysis
- Vehicle dynamics testing
- Rapid control prototyping and HIL applications

## CompactRIO Specifications

| Parameter | Specification | Units |
|---|---|---|
| **Physical/Environmental** | | |
| Dimensions (4-Slot System) | 179.5 by 88.1 by 88.1 (7.07 by 3.47 by 3.47) | mm (in.) |
| Weight (4-Slot System) | 2.55 (5.63) | kg (lb) |
| Temperature Range | -40 to 70 | °C |
| Shock Rating | 50 | g |
| Vibration Rating | 5 | g |
| **I/O Modules** | | |
| Channel Density (Channels per Module) | 4, 6, 8, 16, or 32 | Channels |
| Analog Resolution | 12, 16, or 24 | Bits |
| Maximum Analog Input Rate | 800 | kHz |
| Analog Input Range | ±.08 to ±60 | V |
| Analog Input Signal and Sensor Types | Voltage, current, thermocouple, RTD, strain, load, acceleration, sound, fuel cell, CAN | – |
| Maximum Analog Output Rate | 333 | kHz |
| Analog Output Range | ±10 (±20) | V (mA) |
| Digital Logic Levels | 5 (TTL), 12, or 24 | V |
| Maximum Digital I/O Speed | 30 | MHz |
| Isolation (Withstand) | 2,300 | $V_{rms}$ |
| Removable Nonvolatile Storage | up to 20 | GB |
| **Real-Time Controller** | | |
| Dual DC Supply Inputs | 9 to 35 (on power-up) 6 to 35 (during operation) | V |
| Typical System Power Consumption | 7 to 10 | W |
| Built-In Nonvolatile Storage | up to 512 | MB |
| Serial Port | RS232 | – |
| Ethernet Port | 10/100 | Mb/s |
| **Reconfigurable FPGA Chassis** | | |
| I/O Module Slots | 4 or 8 | Slots |
| FPGA System Gates | 1 or 3 | M |
| Maximum Analog Control Loop Rate | 200 | kHz |
| Maximum Discrete Control Loop Rate | 10 | MHz |

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BY BENOIT SCHILLINGS • TROLLTECH

# Tapping Linux as an application framework for consumer electronics

IN THE HIGHLY COMPETITIVE CONSUMER-ELECTRONICS INDUSTRY, PRODUCT LIFE CYCLES ARE NOTORIOUSLY SHORT, AND DOWNWARD PRICE PRESSURES ARE CONSTANT. AS A RESULT, ELECTRONICS MANUFACTURERS MUST PRODUCE CONSUMER DEVICES FASTER THAN EVER AND REDUCE OVERALL COSTS AND TIME TO MARKET.

Consumers today have demonstrated an insatiable appetite for new electronic gadgets—from mobile phones to media players to car navigation systems. At this year's International Consumer Electronics Show alone, consumer-electronics manufacturers unveiled more than 20,000 new products. Consumers are forever raising the bar of expectation for electronic devices, demanding that companies be more responsive to their needs. It's no wonder that a continuous drive toward innovation characterizes the electronics industry, more than any other. To beat the competition in this business environment, electronics manufacturers must keenly focus on product design and developing innovative devices that are relevant and that resonate with consumers.

Although many consumers continue to think of electronic devices simply in terms of the outward-facing physical structure and style of these hardware platforms, the most innovative and successful products on the consumer-electronics market owe much of their success and popularity to the software component for their ingenuity and differentiation. When looking at the development costs for embedded devices, software remains the single most expensive portion and most difficult system component to manage. Without question, software—not hardware—has emerged as the dominant factor in the cost, time to market, and risk of the product development of electronic devices.

## EXPONENTIAL CHANGE

Developers of embedded devices have traditionally created their own in-house software, which was relatively simple and targeted increasing the performance of these stand-alone devices. They essentially created devices with simple, single-function applications and hardware-centric designs, which they often built on single-processor architectures. However, that approach has changed significantly over the last few years. A trend toward growing software complexity


Figure 1 Linux mobile-development devices, such as Trolltech's Qtopia Greenphone, allow you to create applications.

characterizes today's embedded devices, in which embedded software represents the bulk of the development cost and schedule. In the past, developing software from scratch for each embedded-system project was the norm. This do-it-yourself model was straightforward and worked well for many years. Now, that old way of embedded programming has given way to the need to reuse software and build on software using commercial third-party applications.

The mobile and wireless market is one of the key drivers of consumer electronics. These days, it's not uncommon for smart phones to have millions of lines of software code. (For more on smart phones, see this issue's cover story, "Mobile makeover," on pg 54.) Given this level of complexity, it's not surprising that many electronics manufacturers now employ more software engineers than hardware engineers. After all, software makes a consumer-electronics device more flexible and usable, and the user interface, which the software supports, ultimately has the most impact on the quality of the user experience.

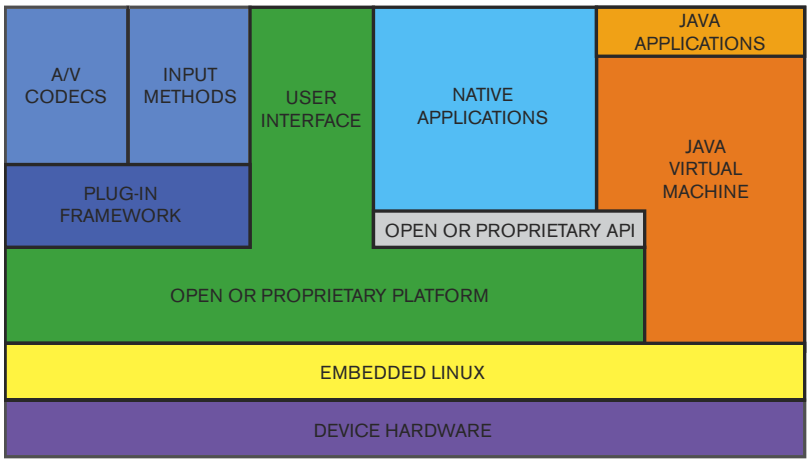


Figure 2 With a platform application framework, developers can create Linux-based devices requiring a rich multiple-application user experience.

Driving the consumer-electronics market is a strong demand to maximize the user-interface experience with applications that require richer content, resulting in devices that have greater software complexity. Nevertheless, an electronic device can have all the functions in the world, but usability is the feature that differentiates a successful product from an unsuccessful one. Having the software-development tools to create a high-quality experience is critical to creating devices that will be successful in the market.

**HAVING THE SOFTWARE-DEVELOPMENT TOOLS TO CREATE A HIGH-QUALITY EXPERIENCE IS CRITICAL TO CREATING DEVICES THAT WILL BE SUCCESSFUL IN THE MARKET.**

## THE LINUX SOLUTION

Because manufacturers now base the differentiation of consumer-electronics devices on the user interface, the need for a flexible application framework is increasingly paramount to meet requirements. The problems for electronics manufacturers are how to continue to attract consumers with enticing new features for their devices, manage the development process, minimize risks, and handle cost and time-to-market constraints. Selecting a software platform is the most important decision a consumer-electronics manufacturer makes in the design process. Manufacturers are increasingly looking to Linux as a platform on which to standardize development, significantly cutting cost and time to market and retaining control over the features and functions of their devices. Linux has emerged as a mainstream technology in the embedded-system world and is the fastest growing operating system in the mobile-device market. The choice to go with Linux and the tools that support it has profound implications for the electronics industry, which has—with good reason—adopted Linux for mobile phones, PDAs, and other consumer devices.

Open-source Linux is robust, powerful, fast, secure, and free. The open-Linux standards are widely available, support reuse, and provide increased compatibility with technologies from other vendors. These tangible benefits from Linux represent an opportunity for consumer-electronics manufacturers to speed their product-development efforts and to provide devices to the market that are both low-cost and easy to use.

Independent research company Venture Development Corp (www.vdc-corp.com) has forecast that the market for embedded-software services for Linux-based devices will continue on an upward trend through 2007. In a recent report, VDC notes several factors, including demand from developers for access to and control of source code, which the open-source software model permits, helping to drive demand for Linux in the embedded-system market. VDC also notes developers' demand for royalty-free runtime software.

A plethora of consumer-electronic devices has incorporated Linux. Leading Chinese telecom manufacturer and wireless provider ZTE (www.zte.com) recently announced the advanced Linux-based e3 smart phone, which most in the industry consider one of the most important smart-phone projects in China. Motorola's (www.motorola.com) A760 smart phone in 2003 was the first handset from the company to use Linux, making the open-source operating system the cornerstone of Motorola's software strategy for mobile devices.

Stuffing a cubic meter
of features into a cubic centimeter
of device requires flexible thinking.

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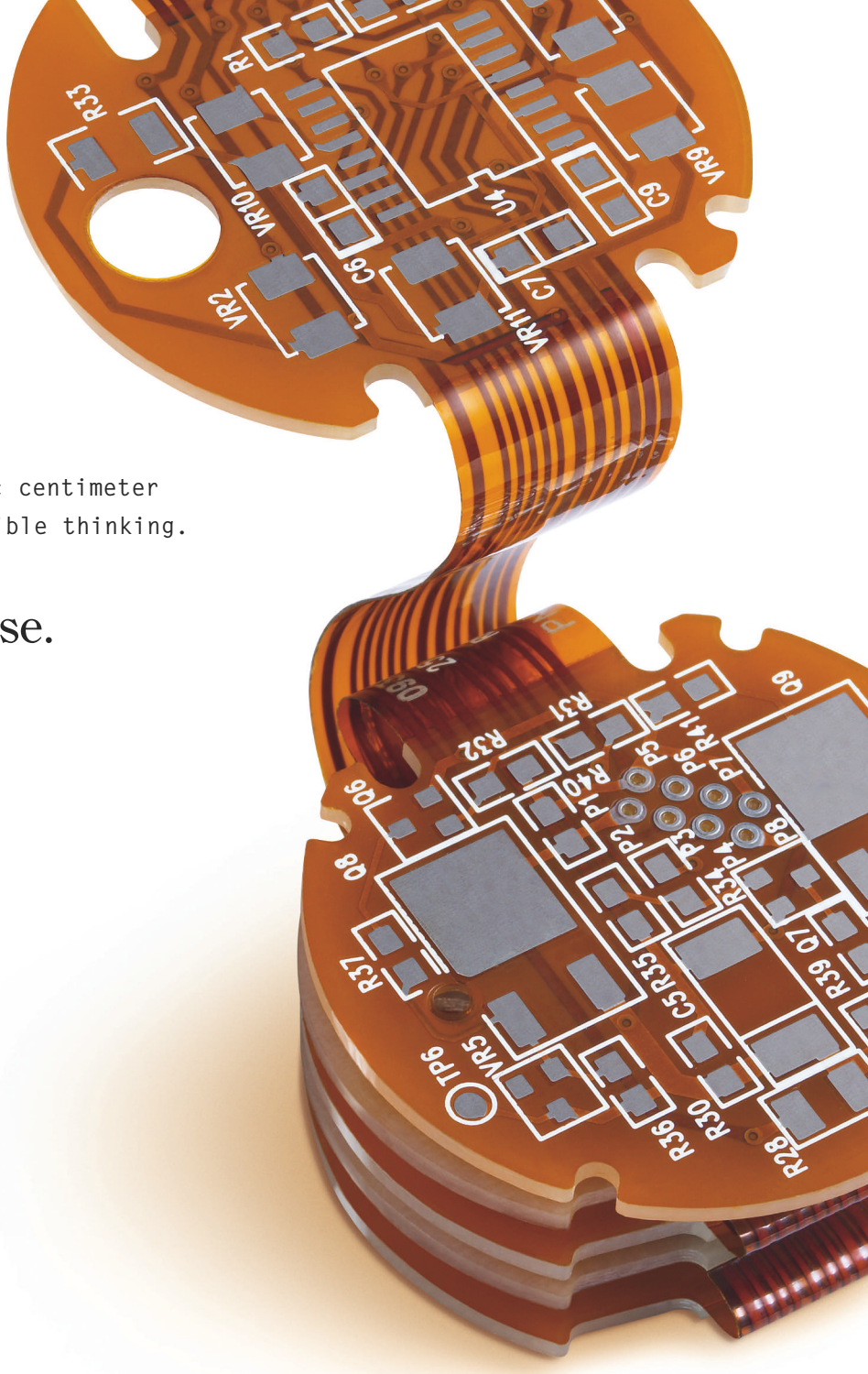
# Optimize.

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Scores of other leading electronics manufacturers have followed suit, lending credibility to Linux (**figures 1** through **3**).

## INNOVATE AND DIFFERENTIATE

With full source code and documentation available, developers working with embedded Linux can easily modify and integrate other technologies to create distinctive electronics devices, freeing them to focus on value-adding innovation rather than on maintaining software. However, using Linux as a kernel is insufficient for manufacturers to truly innovate and differentiate products. Application developers must use an application framework that includes a powerful, rich, and fully documented API (application-programming interface). An API provides a defined method for developing application software, greatly simplifying software development and reducing development cost and time.

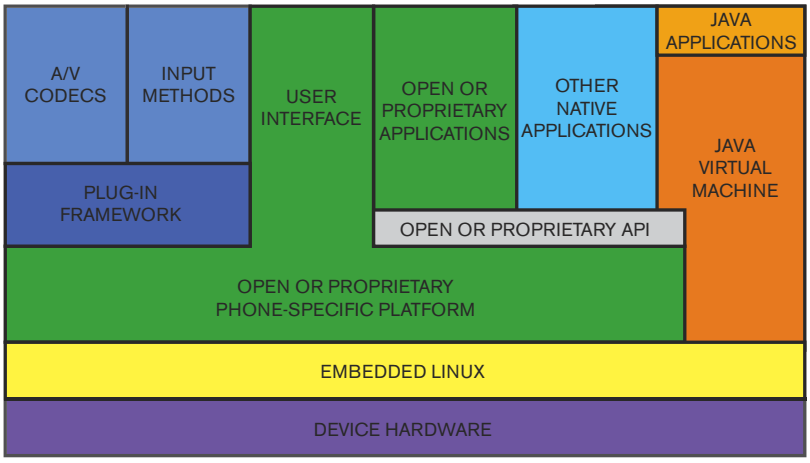


Figure 3 Some application platforms and user interfaces target Linux-based mobile phones.

Hardware-independent APIs enable consumer-device manufacturers to write an application once and deploy it across many platforms—an important feature. When it comes to consumer devices, manufacturers are constantly changing the hardware. Apple (www.apple.com) has changed its successful iPod hardware at least five times since launching in 2001. October 2005 marked the release of the fifth-generation iPod model. By the same token, consumer-electronics manufacturers can't afford a situation in which their software implementation has hardware limitations. Having minimal hardware dependencies that can run unchanged on most standard embedded-Linux setups is optimal, but being able to take advantage of hardware-specific accelerations is also beneficial.

For instance, application frameworks must dynamically take advantage of graphics acceleration, or availability of multiple CPUs. In other words, these frameworks must provide a good abstraction for the hardware without compromising the efficient use of hardware resources. A framework should make it easier to take advantage of the full potential of the hardware, especially in a case of multiple hardware platforms. Device makers need a robust, customizable development platform for creating complex-application devices that embedded Linux powers. This application framework should include a comprehensive set of libraries and graphical tools to help organizations quickly and cost-effectively create embedded-Linux-based products. Linux and this kind of open-source-development platform can reduce fragmentation and the lifetime costs of divergent product lines. In addition, the application framework should build on the security features of Linux to protect the integrity of devices and the network when downloading and running native applications.

A cross-platform application framework should also offer a well-defined development environment for new features, including input methods, fonts, modem drivers, media codecs, and other facilities. It must also include pre-integrated applications, allowing manufacturers and designers to build feature-packed devices. The trend is to increase the features of devices and lower the per-unit cost. Device manufacturers are competing to create products that incorporate the latest technology that can accommodate media-rich content and bring them to the market before their competitors do. These device manufacturers are in the unenviable position of having to add new cutting-edge features and software to their products and operate under constant pressure to reduce the time for designing, prototyping, testing, and manufacturing these increasingly complex devices.

The market for consumer-electronics devices, in which user interfaces play a critical role in customer adoption, is seeing explosive growth due to Linux and application frameworks that ease and speed up development of these devices. Linux provides manufacturers with a great degree of independence and control—attributes that have quickly led to Linux's becoming a standard platform for device design. EDN

## AUTHOR'S BIOGRAPHY

*Benoit Schillings is chief technology officer of Trolltech, where he is responsible for strengthening the company's ability to quickly bring technologies to market. Previously, Schillings was chief technology officer at Openwave Systems, where he was responsible for the structure, design, and operation of Openwave Phone Suite Version 7. In 2003, he was named Distinguished Engineer for his influential work in the conception of "top-to-bottom" integrated software for mass-market phones. Before joining Openwave, he was a principal contributor in the launching of Be Inc, where he designed, developed, and implemented the technically acclaimed BeOS.*


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BY BORIS LERNER • ANALOG DEVICES

# Application dictates choice: fixed- or floating-point DSP?

CHOOSING BETWEEN FIXED- AND FLOATING-POINT IMPLEMENTATIONS CAN BE DIFFICULT. A COMPARISON OF ONE OF EACH TYPE OF PROCESSOR AND SOME SAMPLE APPLICATIONS HIGHLIGHT SOME OF THE PROS AND CONS OF EACH APPROACH.

Without a doubt, many algorithms can benefit from employing a floating-point implementation. The code can be simpler and take fewer cycles to execute than fixed-point implementations. However, these benefits do not really matter that much to end designers. Fewer designers are coding in assembly language, because compilers are getting better; coding fixed- or floating-point implementations in C takes similar complexity. Designers can write floating-point code for a fixed-point processor in C, but doing so causes a significant performance hit. What matters to end designers is the final system's performance, as well as the cost and time to market.

Today's designers have myriad processors from which to choose. Analyzing and comparing all fixed- and floating-point processors is impractical, so this article compares and analyzes a fixed-point ADSP-21531 Blackfin processor and a floating-point ADSP-21375 SHARC. Both of these devices are available for approximately $5 in similar quantities. A first thought might be that, given a similar silicon price, designers should choose the floating-point processor because it can perform the floating-point operations now and in the future should floating-point processing becomes necessary. But a similar price for the silicon does not always translate into a similar price for the end system. For example, performing floating-point operations uses more power than using fixed point for similar tasks. This scenario could mean increased cost in the power-supply design, among other things. In general, each type of application would favor one processor type over the other.

To illustrate, consider applications for a military radar, a mobile television, a professional-audio-effects processor, and an automatic echo canceler in a hands-free portable device. The selection of these applications is not entirely random. These examples illustrate a case in which the fixed- or floating-point processor is a clear winner, in which the answer to the question of which type of processor to use is somewhat unclear and requires more in-depth analysis, or in which the choice can be misleadingly simple. No real-world analysis of this type would be complete without considering the use of on- and off-chip ASIC-hardware coprocessors and FPGAs to offload some of the signal-processing tasks from the DSP. Exploring these options is outside the scope of this article, but such analysis should be part of such a comparison.

## COMPARISONS

Finding the maximal absolute value of a self-ambiguity function lies at the heart of a military-radar application. This function arises as the result of the cross-correlation of a sent test signal with the received echo. The following **equation** gives such a function:

$$A(x,y) = \int_{-\infty}^{\infty} s\left(t - \frac{x}{2}\right)\overline{s\left(t + \frac{x}{2}\right)}\, e^{4\pi i t y}\, dt.$$

This **equation** is the integral of a function against an exponential, and you can compute it using FFT (fast-Fourier-transform) techniques. Floating-point operation is great for computing large FFTs, and no drawbacks exist to using a floating-point processor here. Power is not a major issue as long the heat from the processing can vent so that the processor is not glowing red. The cost of the device is not a major issue, either, because processors constitute a fraction of the cost of the complete system. As a matter of fact, a designer would be unlikely to choose even the sample SHARC device because, for this task, the point is to pack as much processing power as possible into a square inch. Available higher performance floating-point devices with higher processing density would be more appropriate.

Choosing between fixed- and floating-point operation for a mobile-television application is another easy analysis. Mobile TVs have little need for floating-point processing. The bulk of the signal-chain processing resides in standard decoders, such as MPEG-2, MPEG-4, JPEG-2000, and H.264. These algorithms aim for implementation in fixed-point processing; the greater precision and dynamic range that floating-point operation offers is not only unhelpful, but also unusable, because the algorithms are, in general, bit-exact.

Video codecs use some form of DCT (discrete-cosine transform) for the frequency domain. On the surface, floating-point operation appears more suitable for DCT computations. Floating-point computations would produce a more precise

DCT. However, these DCTs target fixed-point arithmetic, and they are bit-exact; more precision is simply wrong here.

Much of the video-codec processing resides in the control code, so no need exists for floating-point operations here, either. Looking at the two processors, the Blackfin's video-acceleration instructions, which accelerate the performance of video algorithms, further strengthen the decision in favor of the fixed-point processor. Additionally, power consumption in the mobile-system market is critically important, so floating-point arithmetic is an expensive luxury. This situation clarifies the decision for the fixed-point processor.

## LESS OBVIOUS

The results of the fixed-versus-floating-point comparison for a professional-audio-effects processor are less obvious. Unlike the mobile-system example, this application has no hard limit on power consumption because audio-effects processors usually plug into a wall outlet. So, unless the processor is so hot that it requires forced cooling—and resultant increased cost—to keep it from melting the solder balls, the comparison of power between the two options comes down to the cost of the power supply.

For example, for an effects processor that has to do a La Scala reverberation, a designer would go to the La Scala opera house in Milan, Italy, and measure its impulse response until the final echo fades away. Implementing this impulse response models the hall's reverberation. Or the designer could cheat and download the already-measured impulse response from a Web site. The impulse response for this example is about 2 sec long. Using a 96-kHz sample rate—the middle ground between 48 and 192 kHz—this scenario translates into 192,000 samples in the FIR-delay line. To precisely implement the reverberation, the effects processor would need to use a 192,000-tap FIR. Directly doing a 192,000-tap FIR would require 192,000 multiplications per output sample. At 96,000 samples/sec, this scenario would mean doing almost 18.5 billion multiplications/sec.

For the total processing requirements that this application needs, the designer must multiply this figure by the number of output channels, add any necessary processing, and allow some performance head room for future expansion. After performing all of these steps, the processing requirements for this example come to approximately 100 billion MACs (multiply-accumulate) operations that need to preserve the 24-bit precision throughout the processing. A designer could have 100 processors performing in parallel, but the resulting selling price and size of the box would most likely have a negative effect on its sales. Thus, some tweaking is necessary, and the tweaks available depend on the choice of processor.

Floating-point processing is good for performing large FFTs, so you can implement the FIR in the frequency domain. One commonly used algorithm for this approach is the overlap-add FFT, which basically computes large FFTs from smaller ones. For this example, choose a 1024-point window for computing an overlap-add FFT. The floating-point processor can perform a 1024-point complex SIMD (single-instruction-multiple-data) FFT in approximately 9200 cycles. Thus, to compute 1024 samples of outputs, the application needs to perform a 1024-point FFT, followed by 1024 complex multiplications, followed by a 1024-point inverse FFT.

AT THIS POINT, THE CHOICE IS BETWEEN THE COST OF DESIGNING A SYSTEM WITH THE FLOATING-POINT PROCESSOR RUNNING AT 10 MHz AND THE COST OF DESIGNING A SYSTEM WITH THE FIXED-POINT PROCESSOR RUNNING AT 60 MHz.

The multiplication operations are equivalent to 4096 real multiplications, which, on this SIMD processor, take 2048 cycles. To compute 1024 outputs requires 9200+2048+9200=20,448 cycles, or about 20 cycles/output. The total number of required cycles increases to approximately 100 cycles/output after adding cycles for the zero padding necessary to perform an overlap-add FFT, accessing external memory to bring in the impulse response's precomputed FFT, and multiplying by the number of channels. At 96,000 samples/sec, the application needs 9.6 million cycles/sec. In other words, this approach consumes only 10 MIPS of the floating-point processor's processing budget.

For the fixed-point processor, the FFT implementation runs into major issues. A 1024-point FFT/inverse-FFT combination has a gain of 1024, or 10 bits. To avoid overflow during the computation of the FFT/inverse FFT, the system must shift down the signal by 10 bits. To preserve the 24-bit resolution, the implementation must keep 34 bits in the arithmetic. Because analog design usually cannot keep up with 24 bits of conversion in its SNR (signal-to-noise ratio), you need to keep 32 bits in the arithmetic to yield 22-bit performance.

A 16-bit fixed-point processor has to perform four multiplications and a few shifts and additions to compute a 32-bit multiplication. It is possible to reduce this number down to three 16-bit multiplications by not computing the last bit, but the math is then 31 bits, and the SNR performance is 21 bits. These values may no longer be good enough for the professional-audio market. In the case of the fixed-point processor, the amount of math increases by a factor of six, and the design needs 60 MIPS of its processing budget. The 60-MIPS budget presumes that this amount is all the processing that needs to take place, which is never the case.

At this point in the comparison, the choice is between the cost of designing a system with the floating-point processor running at 10 MHz and the cost of designing a system with the fixed-point processor running at 60 MHz. At frequencies this low, the dc leakage constitutes a significant chunk of the power, making the frequency difference less relevant and, thus, probably favoring the fixed-point processor. However, as the processing requirements go up, the ac component

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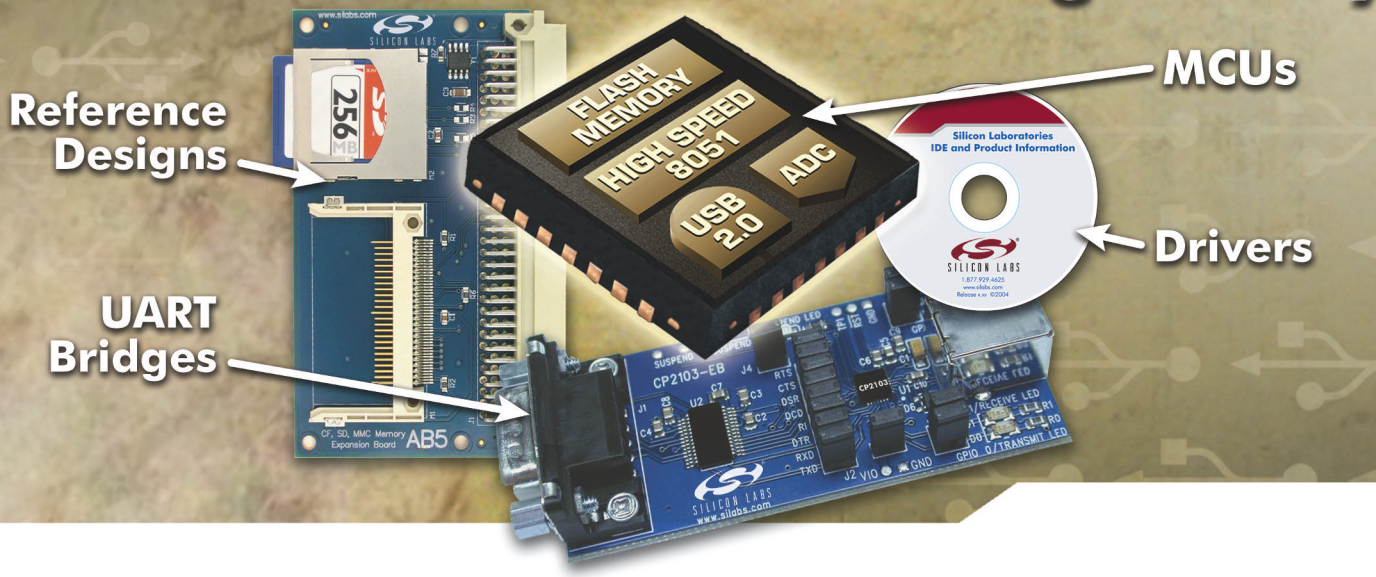


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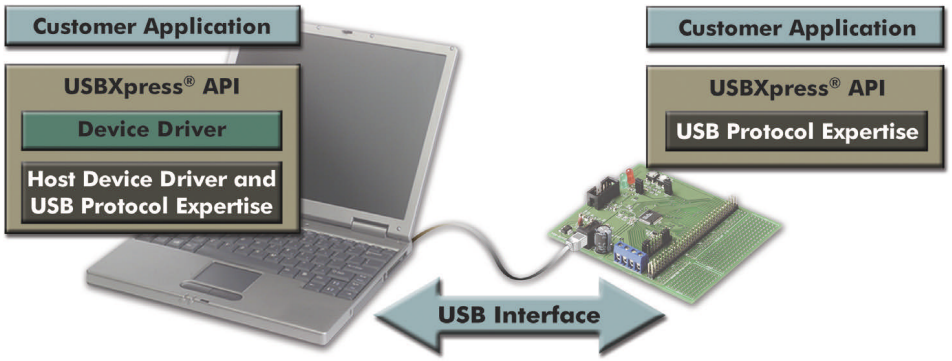


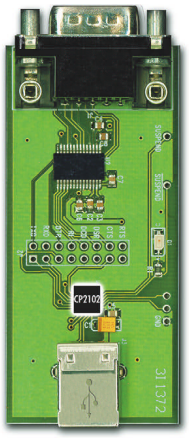

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becomes more dominant, and the factor of six in the frequency starts favoring the floating-point processor. In the extreme case, the fixed-point implementation runs out of MIPS altogether, and the floating-point processor is the correct choice.

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In a different approach, a designer could zero all but the dominant terms and implement an approximation of the required reverberation. So, by keeping 1% of the terms nonzero, this scenario becomes a 1920-tap FIR. An FFT cannot do this task at all because an FFT cannot selectively compute terms; it must compute them all. The designer would directly implement this FIR. This situation means that the system implementation needs to perform 1920 multiplications per output sample. To keep 24-bit precision, multiply the 1920-cycle count by six and divide by two; the fixed-point processor can perform two 16-bit multiplies/cycle, or 5760 cycles/output.

The system needs to support 2-GHz operation after multiplying the 5760 cycles by the number of channels and by the 96,000-MHz sample rate. The system must also allow for the overhead and new features. Zeroing 99.9% of the impulse-response terms enables you to do the design at 200 MHz. This frequency is still higher than that of the floating-point processor, even accepting that the filter's performance begins to suffer.

In real life, professional-audio-effects processors usually include more functions than a reverberation. A designer would have to analyze all the pieces of the processing. In many cases, a floating-point processor consumes less power than a fixed-point processor, in spite of the fact that data-sheet power numbers suggest the opposite.

In a final example, an automatic echo canceler in a hands-free portable device often employs an FFT to compute correlation to the reference signal. It may appear that the previous example clearly makes the point about FFTs; however, an important difference exists. In the last example, the result of the FFT/inverse FFT is the actual signal that goes out to the end user's ears and, thus, has to maintain a high-quality SNR. In the echo canceler, you use the FFT only to compute the time delay of the echo. In other words, it computes the parameter that you then use to compute the actual audio. Thus, a designer could get away with doing an FFT in 16-bit precision, and doing so significantly changes the cycle-count analysis. An additional constraint is that the product is a hands-free portable device. This scenario puts a hard limit on the power budget so that a larger floating-point processor simply has too much dc-leakage power to be a consideration.

In the straightforward cases, it is usually clear which approach is best; however, in grayer areas, this analysis can become complex. Couple this complexity with other considerations, such as ASIC-hardware acceleration to offload some of the processing; ease of programmability, which affects time to market; and maximum dI/dt, which translates into cost for the power-supply decoupling and board layout, and this analysis can become an even greater challenge. EDN

A DESIGNER COULD GET AWAY WITH DOING AN FFT IN 16-BIT PRECISION, AND DOING SO SIGNIFICANTLY CHANGES THE CYCLE-COUNT ANALYSIS.

**AUTHOR'S BIOGRAPHY**

*Boris Lerner is a senior DSP-applications engineer at Analog Devices. His areas of expertise are DSP and communications hardware, software, algorithms, signal integrity, FPGA design, board-level design, and debugging. He received a bachelor's degree and a doctorate in mathematics from the University of Colorado—Boulder and has a master's degree in electrical engineering from the University of Florida (Gainesville).*

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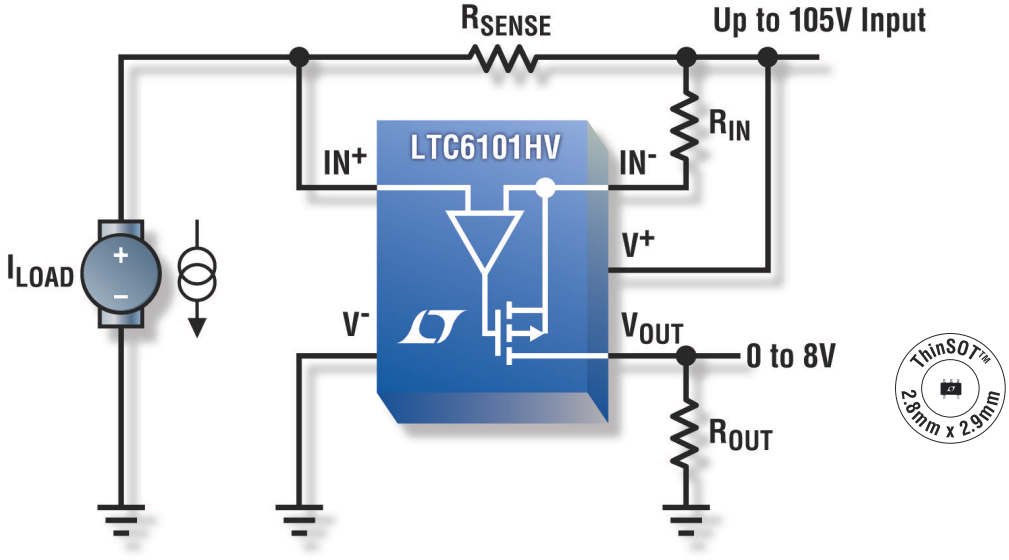


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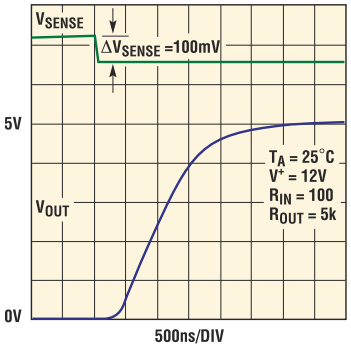


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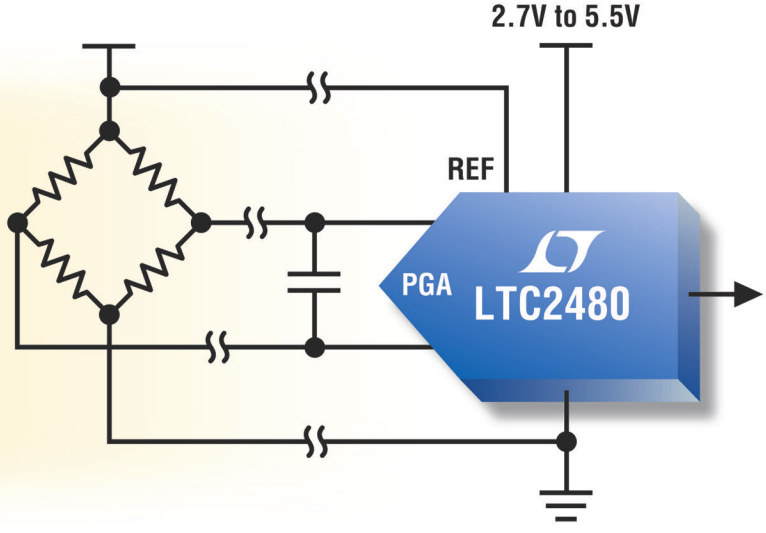


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# PSoC microcontroller and LVDT measure position

Sigurd Peterson, Sig3 Consulting, Aloha, OR

Connecting an LVDT (linear-variable-differential transformer) to a microcontroller can prove challenging because an LVDT requires ac-input excitation and measurement of ac outputs to determine its movable core's position (**Reference 1**). Most microcontrollers lack dedicated ac-signal-generation and -processing capabilities and thus require external circuitry to generate harmonic-free, amplitude- and frequency-stable sine-wave signals. Conversion of an LVDT's output signals' amplitude and phase into a form compatible with a microcontroller's internal ADC usually requires additional external circuitry.

In contrast with conventional microcontrollers, Cypress Semiconductor Corp's (www.cypress.com) PSoC microcontrollers include user-configurable logic and analog blocks that simplify generation and measurement of ac signals. PSoC devices have the unusual feature of being able to generate analog signals without demanding continuous CPU attention. The PSoC's flexible analog and digital blocks can drive an LVDT and measure its outputs without requiring any external circuitry. **Figure 1** shows the complete circuit of the LVDT interface, and **Figure 2** shows

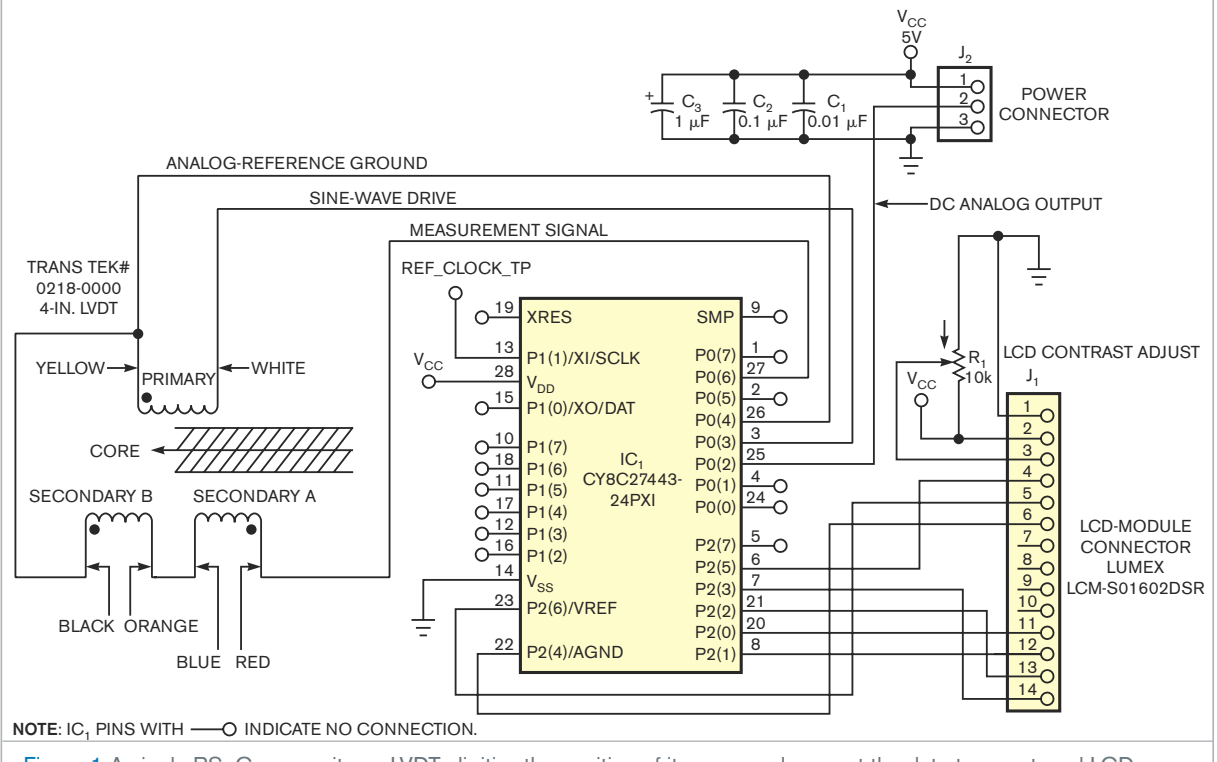



Figure 1 A single PSoC can excite an LVDT, digitize the position of its core, and present the data to an external LCD.

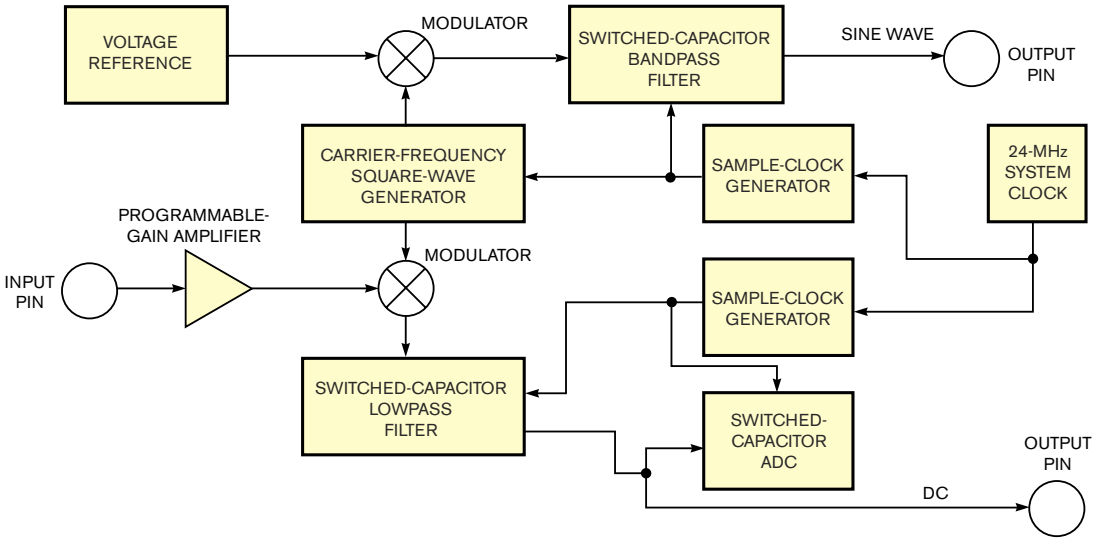



Figure 2 The LVDT-interface circuit requires many analog functions.

the PSoC microcontroller's internal circuit blocks.

The PSoC uses pairs of user-configurable switched-capacitor blocks to implement both bandpass and lowpass filters. You can create a high-quality sine wave by generating a square wave and applying it to a PSoC switched-capacitor filter through a modulator built into the first switched-capacitor block. Passing the square wave through a narrow bandpass filter centered on the square wave's fundamental frequency removes most of the harmonics.

To obtain the highest fidelity sine waveform from a PSoC switched-capacitor bandpass filter, use the highest possible oversampling rate—a factor of approximately 33—or 33 steps per sine-wave cycle. The resultant sine wave is smooth enough to drive an LVDT, which attenuates any residual higher order harmonics. Scaling the PSoC's internal voltage reference with a programmable-gain amplifier provides coarse control over the square wave's amplitude before it undergoes filtering. To compensate for the waveform's dc-offset voltage, an amplifier buffers the 2.6V internal analog-ground reference and drives an output pin that serves as the LVDT's analog-ground return.

The LVDT's output consists of a variable-amplitude sine-wave voltage whose phase angle with respect to the sine-wave excitation voltage undergoes a significant and variable shift that sometimes exceeds 180°. A signal from the LVDT drives one of the PSoC's programmable-gain amplifiers, whose output feeds a switched-capacitor lowpass filter followed by a modulator for synchronous rectification. The rectified signal drives an output pin and one of the PSoC's switched-capacitor ADCs.

Applying the LVDT's output to a synchronous rectifier followed by a lowpass filter produces a dc voltage that can feed an ADC or directly drive an analog feedback-control system. In a PSoC microcontroller, a lowpass switched-capacitor filter connected to an ADC requires that the same sample clock drive both circuits, resulting in a conversion rate for the PSoC's 11-bit delta-sigma ADC that's approximately one-half of the lowpass filter's corner frequency. Synchronous rectification produces a ripple frequency twice that of the excitation frequency and thus is easier to remove with a lowpass filter. Relocating the lowpass filter's corner frequency to one-third of the excitation frequency allows measurements of the LVDT's output to 11-bit resolution with a standard deviation of 1 LSB (least significant bit) or less.

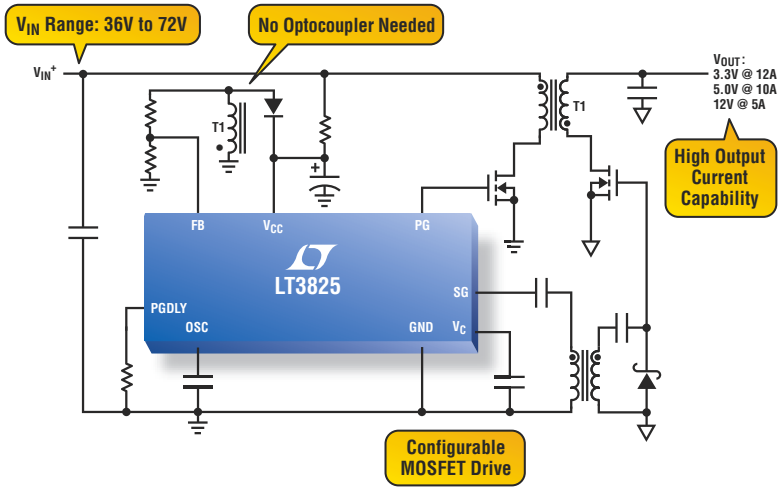
Dividing the PSoC's 24-MHz internal system clock with logic blocks configured as counter chains generates all of the digital clock signals the switched-capacitor analog-circuit blocks require. After power application or a reset, the PSoC's CPU configures all the configured analog and digital blocks and starts their operation. From then on, the hardware excites the LVDT and measures its output at 500 samples/sec without further intervention by the CPU. With the PSoC's CPU running at 12 MHz, processing the ADC's housekeeping activities and interrupts consumes less than 3% of the CPU's resources.

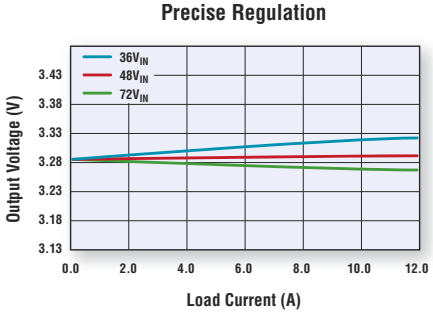
Plenty of the PSoC's resources remain available for calculating the LVDT's position and for displaying the results in text format on an LCD module. Four analog blocks, five logic blocks, and many I/O pins remain available to support a more demanding application. **Figure 3** (next page) shows configurable blocks that are available for adding features. EDN

## REFERENCE

1 "Linear variable differential transformer," *Wikipedia*, http://en.wikipedia.org/wiki/Lvdt.

# Simple 12A Synchronous Flyback

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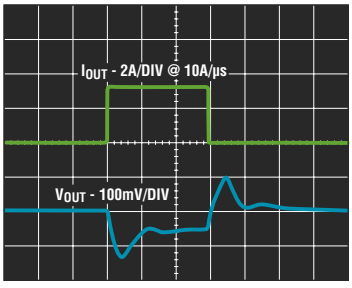


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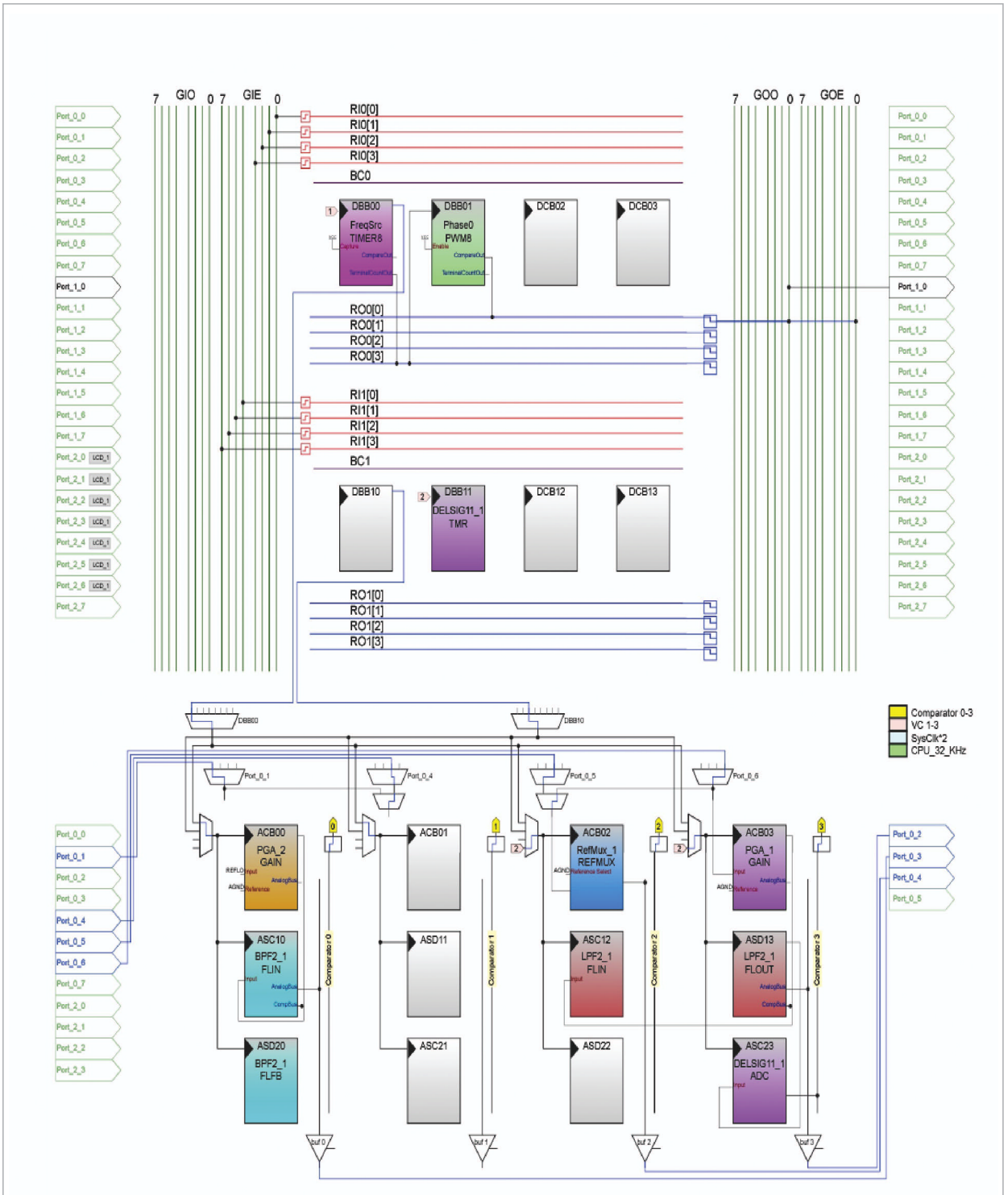


Figure 3 You can use the unlabeled circuit blocks for expansion.

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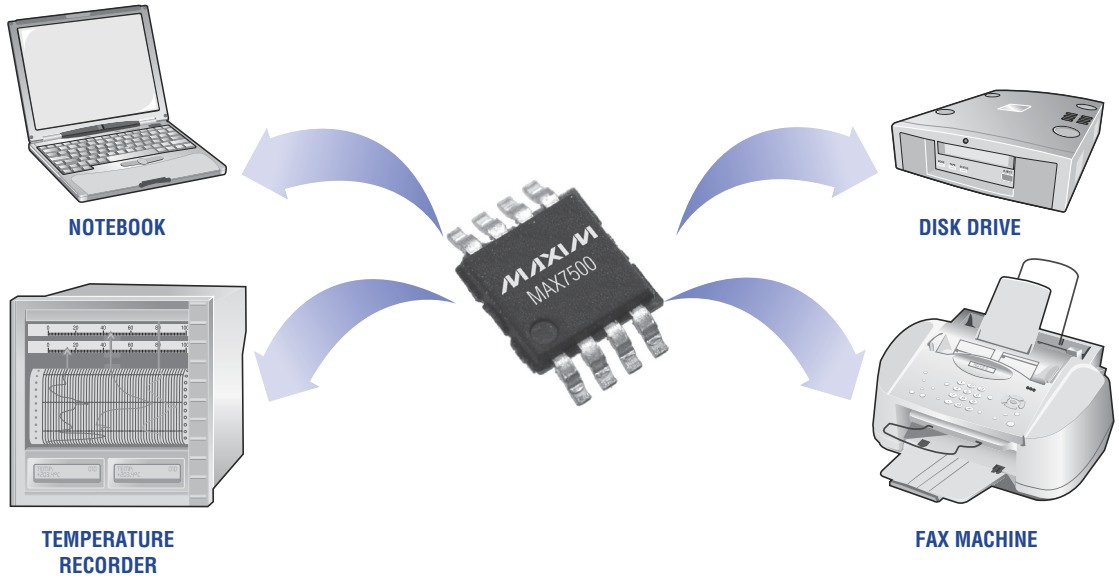


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# Single microcontroller pin senses ambient light, controls illumination

Loren Passmore, Berkeley, CA

As in a previous Design Idea (**Reference 1**), this design uses an LED as a transducer to measure the ambient-light level and to provide illumination. This Design Idea uses the same principle as its predecessor but consists of only one LED, two resistors, one IC, and one 0.1-µF bypass capacitor. This circuit for providing ambient-light feedback requires no additional components. Despite requiring only a few components, the circuit in **Figure 1** offers considerable flexibility because the microprocessor's software controls the LED's brightness and its relationship to ambient-light levels. For night-light applications, one mode turns on the LED when ambient light decreases. Conversely, for power-saving regulation of a portable device's LCD backlight, a second mode turns on the LED when the ambient-light level increases.

You can download **Listing 1**, sample code for this Design Idea, at www.edn.com/061026di1. The code provides 64 levels of PWM (pulse-width-modulated) intensity control over the LED's brightness in either mode. In operation, one of the microprocessor's multifunction pins drives the LED with a PWM waveform for several hundred milliseconds. After the waveform's final cycle, the software switches the microprocessor's pin to input mode and connects the LED to the microprocessor's internal 16-bit sigma-delta ADC. Ambient light illuminates the LED, producing voltage, which the ADC measures, and the microprocessor computes the PWM waveform's parameters for the next series of illumination cycles. The cycle rate's high repetition frequency eliminates any discernible flickering of the LED.

In the **listing**, when the software and ambient-light level specify that the LED should turn off for an extended interval, the CPU goes into a low-power state for 250 msec. During its sleep mode and for a few hundred microseconds while performing ADC conversions, the circuit draws only about 20 µA and thus suits itself well to battery-powered-system applications.

At start-up, the microprocessor stores an initial voltage level, which the LED produces, and uses this value to scale the PWM levels. Shading the LED or moving the circuit into a darker area immediately increases the LED's brightness, which the **listing**'s 64 PWM levels control in small steps. The MSP430F2013's ADC presents input impedance of approximately 200 kΩ. When driving this impedance, an LED occupying a small, 0805, surface-mount footprint generates only a few 10s of millivolts. However, the MSP430F2013's 16-bit ADC resolves the LED's voltage with sufficient resolution to ensure good performance under normal room-lighting levels.

In addition, the MSP430F2013 includes a four-level PGA (programmable-gain amplifier), offering gains of one, four, eight, and 16 to further amplify the LED's minuscule output voltage. The circuit also exploits the microprocessor's onboard low-frequency clock oscillator, which allows low-powered operation without an external crystal. The resultant circuit includes only six components, including a battery. Note: The code can execute on Texas Instruments' (www.ti.com) eZ430 demonstration board without hardware modifications because the board includes an LED connected to port P1.0. EDN

## REFERENCE

1 Myers, Howard, "Stealth-mode LED controls itself," *EDN*, May 25, 2006, pg 98, www.edn.com/article/CA6335303.

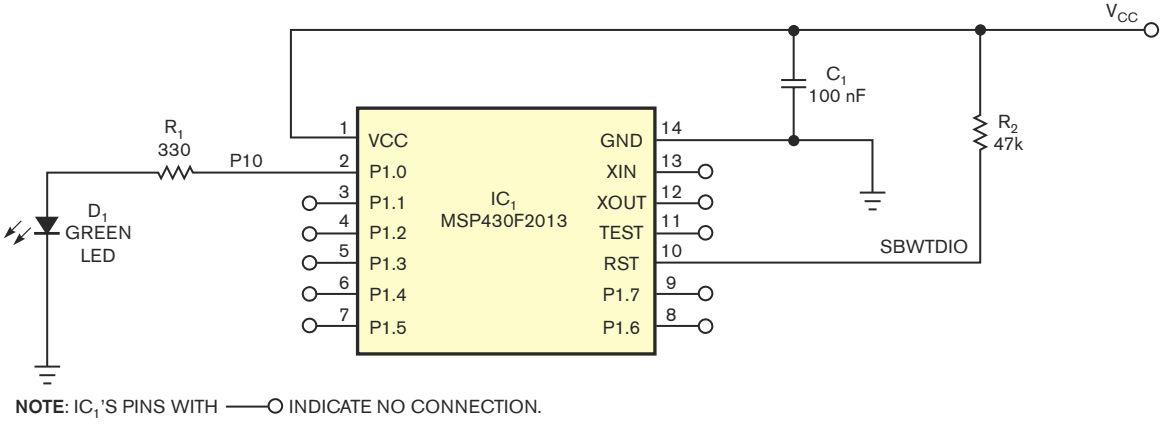


Figure 1 An LED, a microprocessor, two resistors, and one capacitor constitute the entire circuit.

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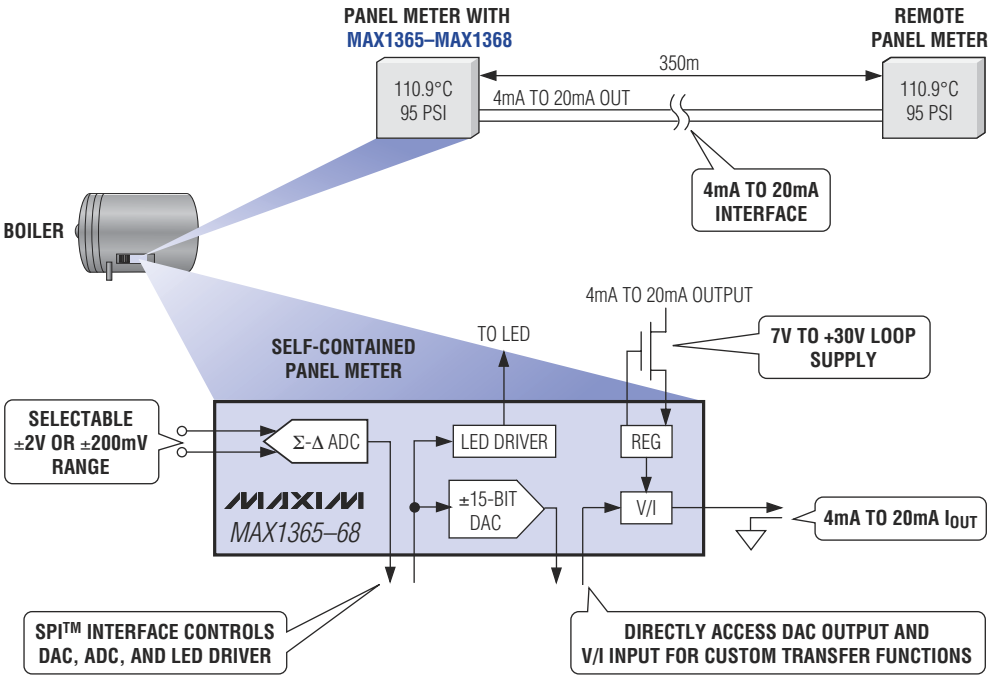


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# Hartley oscillator requires no coupled inductors

Jim McLucas, Longmont, CO

**Editor's note:** *EDN* originally ran this Design Idea in its June 22, 2006, issue. However, due to a number of schematic and textual errors, we have decided to run a corrected, up-to-date version here. We apologize for the errors and hope this version clears up any and all confusion.

Examine a traditional Hartley oscillator circuit, and you'll note its trademark: a tapped inductor that determines the frequency of oscillation and provides oscillation-sustaining feedback. Although you can easily calculate the total inductance required for a given frequency, finding the coupling coefficient, k, poses technical difficulties and may require experimental optimization, also referred to as the "cut-and-try" method. This Design Idea presents an alternative equivalent circuit that allows you to model the circuit before building the prototype.

**Figure 1** shows the Hartley oscillator's equivalent tuned circuit and component values for an 18-MHz oscillator. The mutual inductance is $L_M=k\sqrt{L_1\times L_2}$. For the equivalent circuit, the equations are: $L_A=-L_M$, $L_B=L_2-L_A=L_2+L_M$, and $L_C=L_1-L_A=L_1+L_M$. The rest of the equations for the equivalent circuit are:

$$C_A=-\frac{1}{(2\pi f_O)^2 L_A},$$

$$f_O=\frac{1}{2\pi\sqrt{(L_B+L_C)C}},$$

and

$$C_A=\frac{1}{(2\pi f_O)^2 k\sqrt{L_1\times L_2}}.$$

Unfortunately, a truly equivalent circuit requires a negative inductance, $L_A$. However, for frequencies near the resonant frequency $f_0$, you can replace the negative inductor with a capacitor as (**Figure 1c**), where $C_A$ replaces $L_A$. Note that the equivalent circuit's derivation neglects parasitic winding resistances and capacitances.

**Figure 2** illustrates an oscillator and output buffer using the equivalent circuit. When constructed, the circuit generally performed as expected from an initial Spice simulation. During testing, several components' values required tweaking, and multiple iterations of Spice analysis ultimately yielded the final design.

The oscillator's tank circuit consists of $L_B$, $L_C$, $C_4$, and $C_5$, plus the capacitance provided by the voltage divider $C_6$, $C_7$, and $C_8$—approximately 6 pF, including $Q_1$'s and $Q_2$'s input capacitances and some stray capacitance. The total tank capacitance of 66 pF approximates the calculated value of 67 pF. Capacitors that connect to the tuned circuit feature ceramic-dielectric construction with NP0 temperature coefficients.

Inductors $L_B$ and $L_C$ consist of air-core coils mounted with their axes at right angles to each other to minimize stray coupling. However, vibration affects their inductances, and, in a final design, both should consist of windings on dielectric cores or on toroidal cores, providing that the toroids' temperature coefficients of inductance are acceptable for the intended application.

The information in **Reference 1** provided basic designs for both inductors, and adjusting the spacing of their turns tuned the oscillator to exactly 18 MHz. For a more rigorous design, you can measure the inductors before installation, but parasitic effects may require some adjustment of the inductors.

The capacitive voltage divider, $C_6$, $C_7$, and $C_8$, applies the proper signal levels to $Q_1$ and $Q_2$. Because the divider's effective capacitance as "seen" by the tank circuit amounts to only 6 pF, you can replace the remaining 60 pF consisting of $C_4$ and $C_5$ with a variable capacitor if the design calls for a tunable oscillator. In this example, the output stage consisting of $Q_3$ and its associated components would require modification to provide more bandwidth if the oscillator requires a tuning range exceeding ±2 MHz.

Capacitor $C_3$ bootstraps $Q_1$'s Gate 2 to its source, which provides additional gain and reduces $Q_1$'s Gate 1 input capacitance below its already-low value of approximately 2.1 pF (**Reference 2**). An 8.3-µH inductor, $L_2$, of less than 2Ω dc resistance connects to $Q_1$'s source and presents a relatively high impedance at 18 MHz and provides a dc path from $Q_1$'s source to ground through $R_3$. At 18 MHz, $L_2$ has an impedance that consists of an inductive reactance of about 940Ω

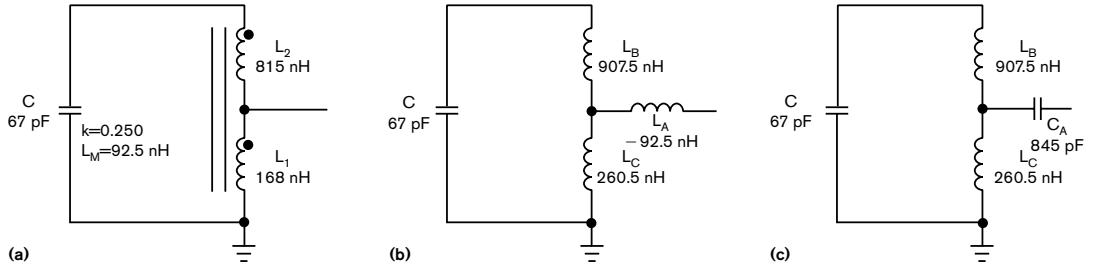


Figure 1 A traditional Hartley oscillator's resonant circuit consists of a tapped inductor and resonating capacitor (a). Allowing for mutual coupling between windings produces an equivalent circuit containing a negative inductance (b). Replacing the negative inductance with a capacitor yields an easily modeled equivalent circuit (c).

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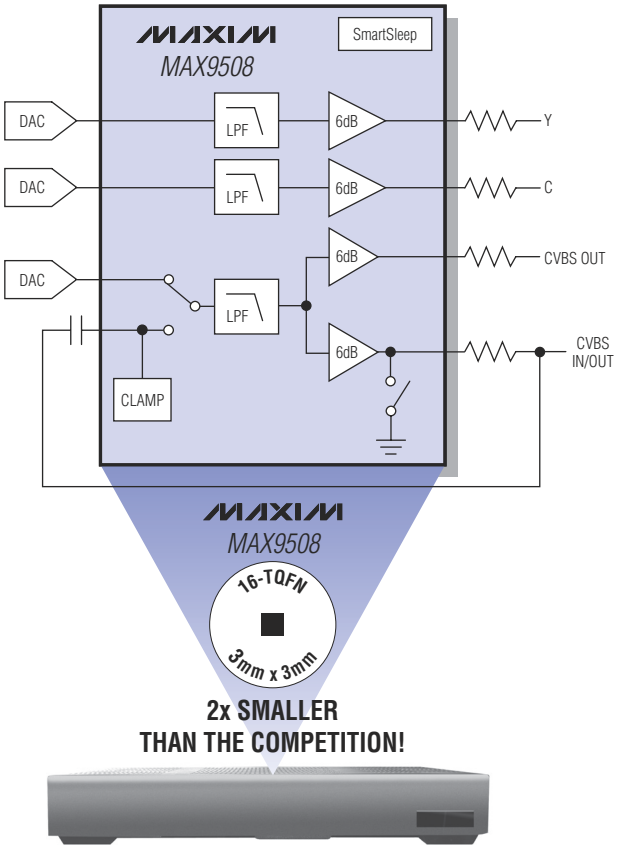


| Part | No. of Inputs | No. of Outputs | Supply Voltage (V) | Filter Passband (MHz at ±1dB) | SmartSleep | Additional Features | Package Size (mm x mm) | Price† ($) |
|---|---|---|---|---|---|---|---|---|
| MAX9508 | 3 | 4 | +3.3 | 6.75 | Yes | Bidirectional CVBS | 3 x 3 | 0.59 |
| MAX9512 | 2 | 4 | +3.3 | 6.75 | Yes | Y/C mixer | 3 x 3 | 0.59 |

†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

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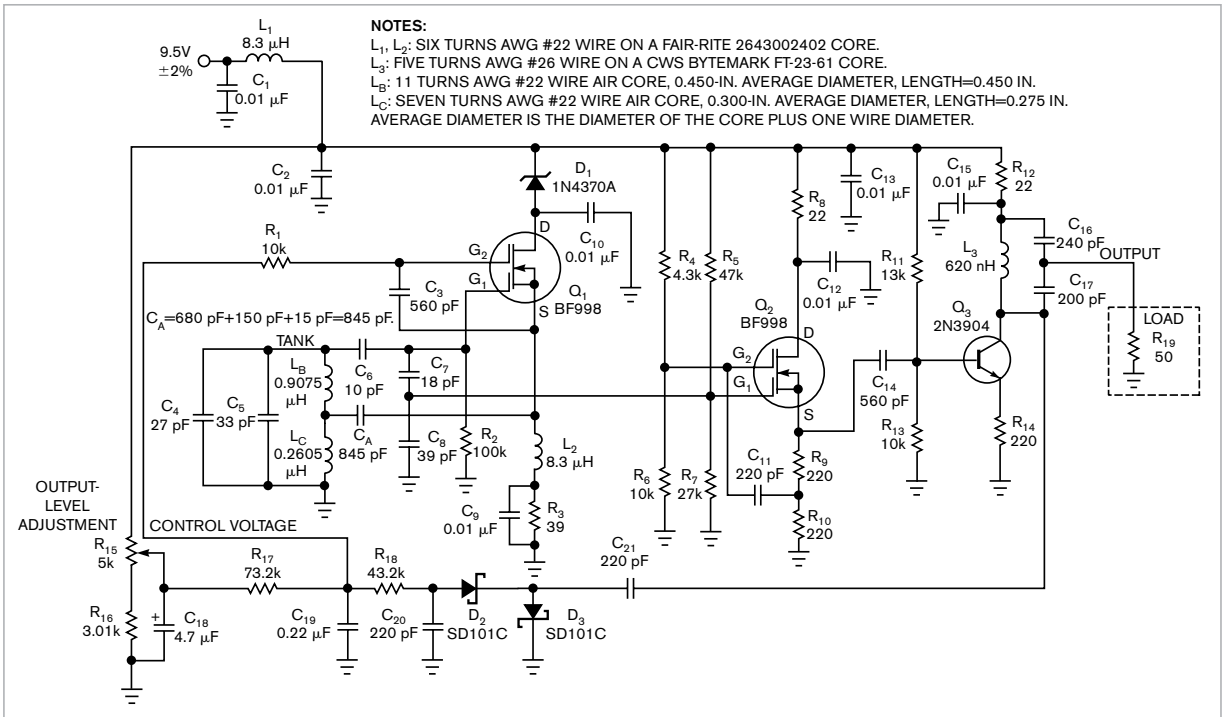


Figure 2 This buffered-output, 18-MHz oscillator features a resonant circuit that doesn't rely on mutual coupling for operation.

in parallel with a resistance of about 3.5 kΩ, which results in a very-low-Q choke. Provided that its inductance and reactance approximate $L_2$'s original values, you can substitute a physically smaller inductor for $L_2$. Inductor $L_1$'s properties are less critical, but it should present a low Q of 4 to 6 and a dc resistance of approximately 5Ω or less. You can use a standard-value choke for $L_1$ if it meets these requirements.

Source follower $Q_2$ drives the output stage, which uses a pi-matching network to transform the 50Ω output load to 285Ω at the collector of $Q_3$. Bootstrapping $Q_2$'s Gate 2 by one-half of the stage's output voltage increases the source follower's gain and dynamic range and reduces its input capacitance.

You can use potentiometer $R_{15}$ to adjust the circuit's output level from about 0.9V p-p to approximately 1.5V p-p across a 50Ω load. At a constant room temperature of about 23°C, the frequency remains stable, and the circuitry that controls output level remains stable even with no load on the output. For a fixed-frequency application, the output circuit's loaded Q of 4 provides adequate bandwidth to eliminate retuning of the output circuit for small changes in frequency.

To set the output level to a safe maximum, connect a 50Ω load to the output, and then adjust the output to 1.5V p-p. The drain-to-source voltage applied to $Q_1$ will remain at a safe level for all loads from 50Ω to no load, even though the output-voltage level increases as the load resistance increases. To avoid exceeding $Q_1$'s specified maximum 12V drain-to-source-voltage rating, do not exceed an output-voltage setting of 1.5V into a 50Ω load. Note that zener diode $D_1$ reduces $Q_1$'s drain voltage to provide an additional safety margin.

In a previous Design Idea, an operational amplifier and a diode-rectifier circuit set the oscillator's gain through a control voltage applied to $Q_1$'s Gate 2 (**Reference 3**). In this design, a simple passive circuit serves the same purpose. A portion of the signal at $Q_3$'s collector drives a voltage doubler consisting of $D_2$, $D_3$, $C_{20}$, and $C_{21}$. Part of the negative voltage developed by the voltage doubler drives the junction of $R_{18}$ and $C_{19}$, the control-voltage node, which also receives a positive voltage from variable resistor $R_{15}$ through $R_{17}$, and the resultant voltage sets the output signal level. At start-up, only a positive voltage is present at $Q_1$'s Gate 2, and $Q_1$'s maximum gain easily starts the oscillator. When the output reaches a steady state, the control voltage reduces and maintains oscillation at the signal level determined by the output level control. **EDN**

## REFERENCES


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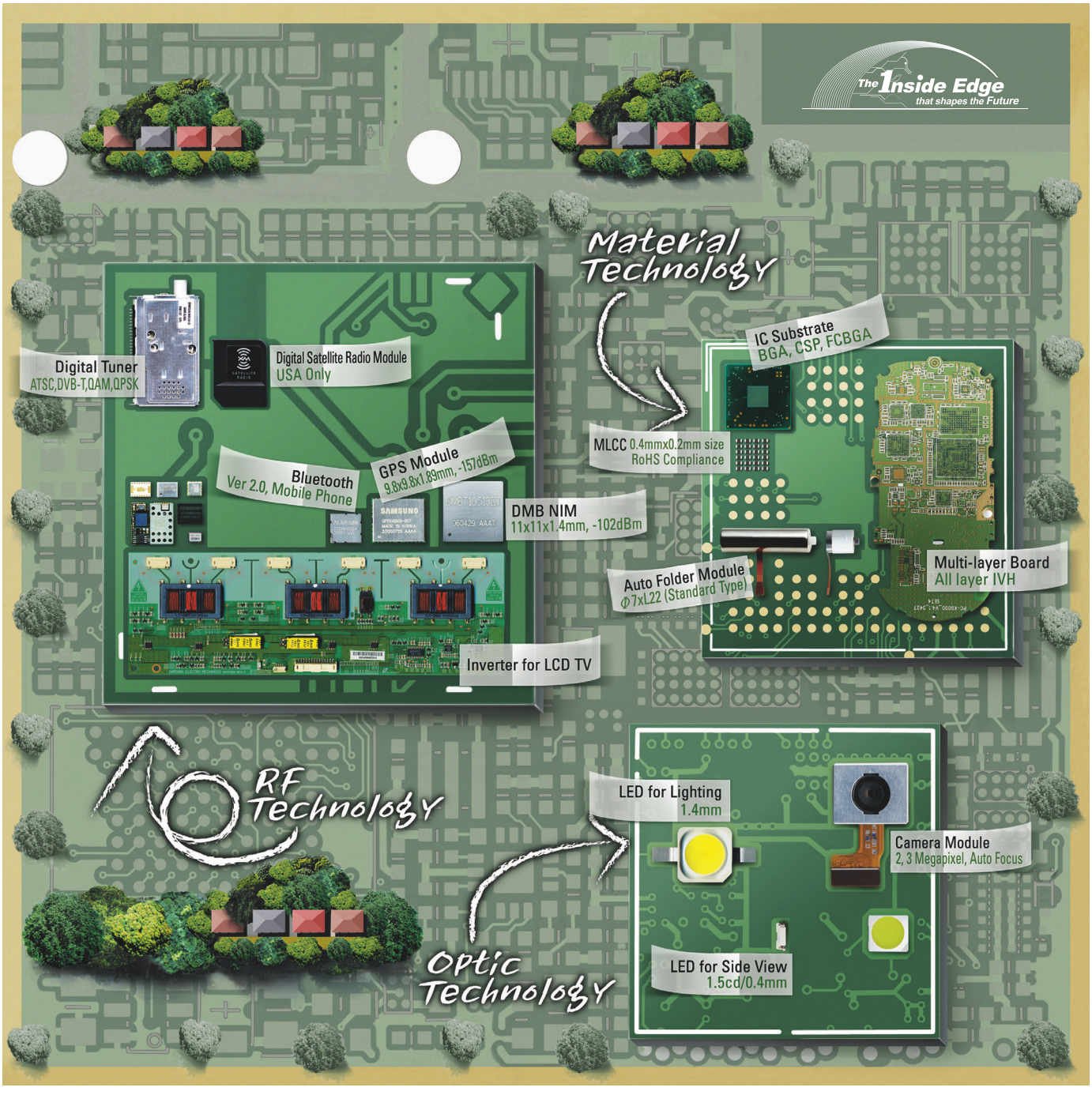
2 "Practical FET Cascode Circuits, Designing with Field-Effect Transistors," Siliconix Inc, 1981, pg 79.

3 McLucas, Jim, "Stable, 18-MHz oscillator features automatic level control, clean-sine-wave output," *EDN*, June 23, 2005, pg 82, www.edn.com/article/CA608156.




# The 1nside Edge that shapes the Future

Samsung Electro-Mechanics (Samsung) has started up production of **LEDs** for lighting as well as mobile phones, car navigators, PMPs and Note PCs.

**SB Byun** (sbbyun@samsung.com, 949-797-8054)

Samsung has brought out 2, 3 Megapixel **camera module** with auto focus function.

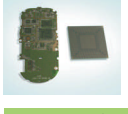
**JIM Park** (jimpark@samsung.com, 847-549-9421)

Samsung has produced digital tuners compatible with all broadcasting signals worldwide, for TV, Set-top boxes and mobile phones, as well as a variety of micro-sized RF components, **Bluetooth, wireless LAN, GPS Module, FEM,** etc., that support the portability of mobile devices.

**JS Han** (han.jungsuk@samsung.com, 201-229-6096)

Samsung has completed development of world's first 0402(0.4X0.2mm) **MLCC**, as thin a human hair, which uses copper nickel, palladium as internal electrode material. Specifically, 0402 Cu MLCC has better high frequency performance than others.


**Peter Kang** (semksk@samsung.com, 949-797-8017)



Samsung has offered **multi-layer boards** named,'SAVIA™(Samsung Any Via)', which have all-layer IVH characteristics and **Flip Chip substrate.**

**Wes Sohn** (wansohn@samsung.com, 480-592-0180)

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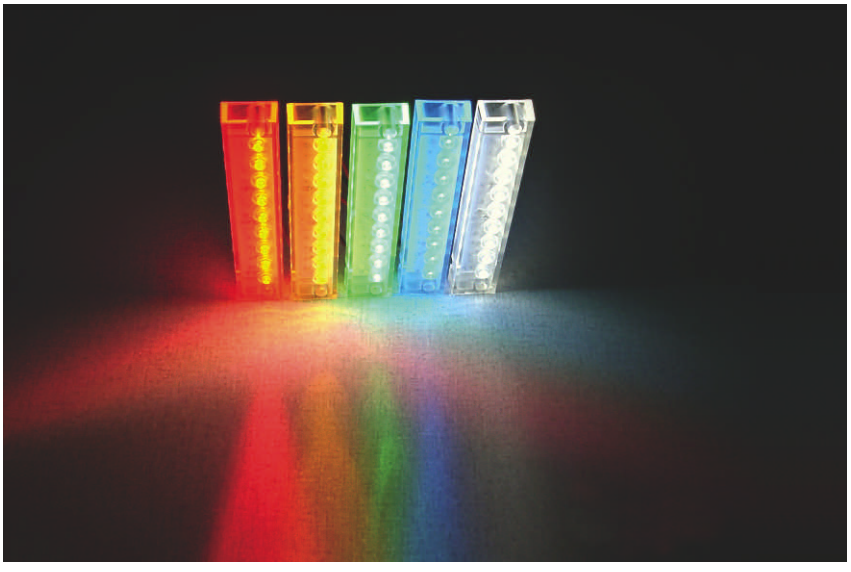
## OPTOELECTRONICS/DISPLAYS



### Low-voltage LED assembly suits emergency applications

Targeting the emergency and security industry, this environmentally sealed LED-lamp assembly meets the color and brightness levels for safety kiosks on college campuses and hospital parking lots. The device comprises LED arrays and potted mounting lenses, making it resistant to moisture and dirt. Operating at 12 to 26V ac and 12 to 16V dc, the assembly features a set of transistors that allows the arrays to operate at any voltage in the desired range. Options include the vendor's standard 5-mm, high-intensity, 20°, indium-gallium-nitride, white LED. The LED assembly costs $34.46 (1000).

**DDP, www.datadisplay.com**

### Surface-mount LEDs range the visible spectrum

This surface-mount-LED family of illumination devices creates colors along the entire visible spectrum. These discrete RGB LEDs come in a variety of sizes and viewing angles and feature modules with flat and domed lenses. Available in a 3.5×3×1.4-mm package with a 110° viewing angle, the LED family costs 95 cents (10,000).

**Optek Technology, www.optekinc.com**

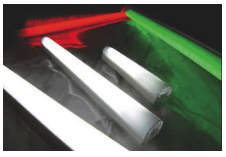
### Boost converter drives as many as 10 LEDs

Driving as many as 10 LEDs, the high-voltage CAT4238 boost converter uses a low-noise, high-frequency switching scheme. Integrated features eliminate the need for external components for soft-start and overvoltage protection, reducing noise and board-space requirements in midsized to large LCD-panel-backlighting applications. The driver operates at a fixed 1-MHz frequency. Available in an ROHS (reduction-of-hazardous-substances)-compliant SOT23 package, the CAT4238 costs 78 cents (10,000).

**Catalyst Semiconductor, www.catsemi.com**

### LED-tube lights save energy

The milky-frosted lens of the TBL-3xxF series of sealed-tube LED light strips provides a diffused illumination. The tubes use less energy and lower voltages than neon lights. They come in 6000K pure-white and 3000K warm-white colors and operate at 12V. Available in 6-, 12-, 24-, and 48-in. lengths, the TBL3xxF series devices have prices ranging from $26.95 to $108.35, depending on length.



**LEDtronics, www.ledtronics.com**

### LED drivers come in small packages

Driving high-brightness LEDs in backlighting applications for cellular phones, digital cameras, and MP3 players, these white-LED drivers claim 90% efficiency. Powering two to five white LEDs for LCD backlighting, the NCP5010 provides a 22V power supply, 84% efficiency, a 1-μA shutdown current, and the ability to operate on a 2.7 to 5.5V input voltage. Features include true cutoff, short-circuit, and overvoltage protection and undervoltage

LINEAR TECHNOLOGY

DESIGN NOTES

# Power Supply Sequencing Made Simple – Design Note 401

Bob Jurgilewicz

## Introduction

System designers face a number of problems when it comes to controlling multiple power supplies. Turn-on and turn-off characteristics, supply monitoring, fault management and reset generation are a few issues that affect both the short term system performance and long-term reliability. Design is further complicated by a process that often puts final decisions about supply requirements at the end of the design phase. So, a good supervisor/control solution allows for easy design and adjustment anywhere in the design process.

Firmware solutions place a daunting hurdle directly in the critical path of the design. Every change involves software engineers, a load of testing and worst of all, waiting. Loading code during production is time consuming and costly.

A better solution uses hardware, but easy-to-change, relatively inexpensive hardware. How about generic reusable circuit blocks that are added early in the system design with little regard to the final specific power requirements? The existing blocks are left unfinished, simply waiting for passive component values to be determined. When final decisions about the power supplies' operating specifications are determined, calculate the values for a few passive components and populate the empty spaces in the circuit. Fortunately, such a solution exists.

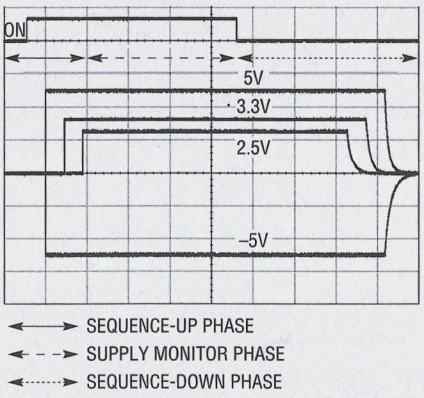



**Figure 1. Sequencing Application Waveforms**

The LTC2928 is a 4-channel cascadable power supply sequencer and high accuracy supervisor. Multiple LTC2928s can be easily connected to sequence an unlimited number of power supplies. Cascade action is via a single pin connection and is functional during sequence-up and sequence-down operations. Sequencing thresholds, order and timing are configured with just a few external components, eliminating the need for PC board layout or software changes during system development. Sequence outputs control supply enable pins or N-channel pass gates. Precision input comparators with individual outputs monitor power supply voltages to 1.5% accuracy. Supervisory functions include under and overvoltage monitoring and reporting as well as reset generation. The reset output may be forced high to complement margin testing.

Application faults, whether generated by the LTC2928 or communicated by a host, can shut down all controlled supplies. The type and source of faults are reported for diagnosis. Individual channel controls are available to independently exercise enable outputs and supervisory functions. A high voltage input allows the LTC2928 to be powered from voltages as high as 16.5V. A buffered reference output permits negative power supply sequencing and monitoring operations.

## Three Phases of the Power Management Cycle

A complete power management cycle is divided into three phases as shown in Figure 1. The sequence-up phase initiates by transitioning the ON pin above threshold with a logic signal or power supply. The controlled supplies sequence-up with user configured order and timing. All supplies must exceed a user defined sequence-up threshold within the configured "power-good" time. If any supply fails to turn on properly, a sequence fault occurs and all controlled supplies are shut down. Once all supplies reach their sequence-up threshold, the supply monitor phase begins.

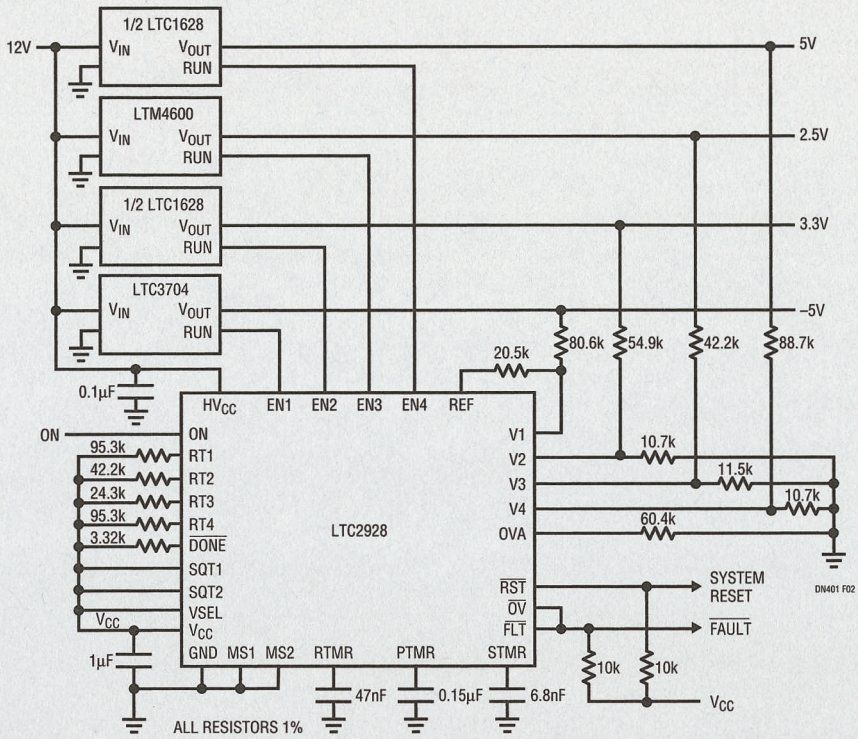



**Figure 2. LTC2928 Application Schematic (component values calculated with the LTC2928 Configurator Tool)**

During the supply monitor phase, the input signals are continuously compared against user configured undervoltage and overvoltage thresholds. The comparators filter out minor glitches coupled to their inputs. If any supply is out of compliance with sufficient magnitude and duration, the reset output ($\overline{RST}$) and/or overvoltage output ($\overline{OV}$) pulls low. Once all inputs are within compliance, the respective monitor output pulls high after the user defined reset delay. Users may select whether or not a fault is generated on the basis of under or overvoltage events. A generated fault shuts down all controlled supplies. Shutting down upon an undervoltage fault is often a critical operation. For example, consider a temporary short on one supply due to a probe slip. Once the short is removed, the supply may recover, but it might do so out of sequence if the other supplies are unaffected. A reset fault shuts off all the supplies, allowing for a new in-sequence start-up procedure.

The sequence-down phase initiates by transitioning the ON pin below threshold with a logic signal or power supply. The controlled supplies sequence-down with user configured order and timing. All supplies must fall below the user defined sequence-down threshold within the configured "power-good" time. If any supply fails to turn off properly, a sequence fault occurs and all controlled supplies are shut down.

## LTC2928 Configuration Software Designs It for You

To make life truly simple, Linear Technology offers free configuration software that calculates all resistor values, capacitor values and required logic connections. The tool also generates schematics and a passive element bill-of-materials. All you need to know are your supply parameters and sequence order. Contact Linear Technology for details.

## Conclusion

The LTC2928 greatly reduces the time and cost of power management design by eliminating the need to develop, verify and load firmware at back end test. System control issues such as sequence order, timing, reset generation, supply monitoring and fault management are all handled with the LTC2928.

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## OPTOELECTRONICS/DISPLAYS

lockout. The NCP5604A and NCP5604B drive three and four LEDs, respectively, at 25 mA of current per LED. A 0.5% current-matching tolerance allows a uniform LED brightness. Peripherals feature a 90% efficiency with a 1-μA quiescent current. Available in an eight-pin, 1.7×1.7×0.6-mm flip-chip package, the NCP5010 costs 67 cents (3000). Available in a WQFN-16 package, the NCP5604A and NCP5604B cost 69 cents and 66 cents (3000), respectively.
**On Semiconductor, www.onsemi.com**

## EMBEDDED SYSTEMS

### Isolated-driver card has overload protection

Targeting the PC/104 bus, the 24-output 4I37 isolated driver can drive solenoids, lamps, and large relays with 28V-dc power-supply voltages. Each output driver features overload protection, clamp diodes, and the ability to sink 1A of current. Organized as two 12-bit ports for faster updating, the outputs provide a 2-μsec switching time. A galvanic isolation between logic and power circuitry prevents the return current from interfering with CPU logic and also allows the use of loads with a common positive ground. The 24 bits can be read back, allowing you to use unused outputs as inputs and to verify output switching. The 4I37 costs $112 (100).
**Mesa Electronics, www.mesanet.com**

### LCD-panel computer features a four-wire resistive touchscreen

With an 8.4-in. LCD and a 3.5-in. embedded board, the LCD-panel computer incorporates a VIA Eden 667-MHz processor, three RS-232 ports, and a four-wire resistive touchscreen. Featuring a built-in VGA controller with as much as 32 Mbytes of shared memory for display, the device has a 144-pin SO-DIMM socket with as much as 512 Mbytes of memory capacity. The device has an onboard CompactFlash Type-1 socket and a 16-bit PC/104 extension connector, with an optional 2.5-in. hard-disk drive and PCMCIA for wireless applications. The LAN uses a Realtek 8139 C PCI plug-and-play BaseT Ethernet controller. The ARP-2608AP LCD-panel computer costs $1000.
**Arista Corp, www.aristaipc.com**

### Two wireless modules are FCC- and ETSI-certified

Adding to the vendor's wireless-product family, the 1-mW LPR-2400 and 65-mW LPR2400ER RF adapters operate at 2.4 GHz. These devices comply with the IEEE 802.15.4 standard and have FCC (Federal Communications Commission) and ETSI (European Telecommunications Standards Institute) certification, making them suitable for industrial and factory applications. The LPR2400 and LPR2400ER measure 0.8×1.2 in. and 0.8×1.2 in. and cost $22 and $36, respectively. Developer's kits are available for $199.
**Cirronet, www.cirronet.com**

### DAP board has simultaneous sampling on many channels

Powered by an Intel Pentium 233-MHz processor, the mid-range DAP (data-acquisition-processor) 5380a/526 board features 16 analog inputs and acquires 14-bit data at 800k samples/sec/channel. The device simultaneously samples eight channels at 625k samples/sec on each channel, providing a 5 million-sample/sec throughput. The DAPstudio Windows application can control and configure any DAP from a PC. The DAP 5380a/526 board costs $3995; DAPstudio costs $199.
**Microstar Laboratories, www.mstarlabs.com**

### Universal serial I/O features four independent ports

The DNA-SL-501, serial-I/O-layer board features four independent, isolated, RS-232, -422, or -485 ports with 1-Mbps maximum data-transfer rates in RS-485 mode. Designers configure the ports using software, allowing each port to have a different configuration. The DNA-SL-501 costs $650.
**United Electronic Industries, www.ueidaq.com**

### Single-board computers use two Dual Core processors

These single-board computers incorporate two ultralow-voltage Dual Core Intel Xeon processors on a 6U, single-slot module. These devices provide four times more processing density per module than single-core Xeon-

# productroundup

## EMBEDDED SYSTEMS

processor-based boards. The Momentum Series CX6-200 6U CompactPCI-based single-board computer features symmetric multiprocessing. The Momentum Series CX6-200 costs $6295.
**Mercury Computer Systems, www.mc.com**

option is available with an IPMI (Intelligent Platform Management Interface)-based bus that is compliant to PICMG 2.9. The CompactPCI Express chassis costs less than $1000, depending on volume and configuration requirements.
**Elma Electronic Inc, www.elma.com**

### Video-acquisition tool captures 30 frames/sec

Able to capture full-frame, 720× 480 video at 30 frames/sec, this frame grabber performs motion detection in three programmable regions with bit rates ranging from 800 kbytes/sec to 10 Mbytes/sec. The device features two synchronized-audio-input channels and an OSD (on-screen display). Linux, QNX, and Windows drivers come with an available Fast Windows stream player. Uncompressed video is available through the PC/104+ bus for previewing. The Sensoray Model 314 MPEG-1/2/4 and the MJPEG frame grabber cost $328.
**Sensoray, www.sensoray.com**

### ROHS-compliant module features eight channels

With a full industrial-temperature range from −40 to +85°C, the ROHS (reduction-of-hazardous-substances)-compliant PCM-COM8-G PC/104 asynchronous communications module features eight channels. Each channel can support RS-232, RS-485, and RS-422 electrical levels. The PCM-COM8-G costs $249.
**WinSystems Inc, www.winsystems.com**

### Four-slot chassis features bottom-to-top cooling

Available in a 19-in. rack-mount or desktop style with horizontally mounted cards, the 4U-tall chassis features a four-slot 3U backplane, 3×75 cfm bottom-to-top cooling, and advanced EMC shielding. It meets NEBS as well as CE and FCC standards. The device features 90 to 264V ac or 48V dc PSU inputs and fixed-mount, plug-in, or N+1 options. A shelf-management

### Processor operates as system controller

Using the 1-GHz MPC7447A or 1.4-GHz MPC7448 Freescale processor, the 6U CompactPCI C2K single-board computer has a PLX PCI 6254 CompactPCI-backplane bridge, allowing it to operate as a system controller or as a peripheral processor card. The device features three Gigabit Ethernet ports, four RS-232/RS-422 ports, four RS-422/RS-485 ports, two 1.5-Gbps SATA ports, and three high-speed USB 2.0 ports. The C2K board computer costs $2790.
**GE Fanuc Embedded Systems, www.sbs.com**

## TEST AND MEASUREMENT

### Upgrade for multimeter features function generator

With a function generator that can source pulses and sine waves at 20V p-p, the SMX2064 DMM (digital multimeter)/LCR (inductance/capaci-

# TEST AND MEASUREMENT

tance/resistance) meter generates pulses in a burst of as many as 60,000 pulses or a continuous signal with 1-µsec resolution. The device also generates 1-Hz to 200-kHz sine waves with 2-MHz resolution. In addition to the function generator, the SMX2064 features a dc- and ac-voltage generator, a current generator, and a frequency counter. The SMX2064 DMM/LCR meter costs $2195.

**Signametrics Corp, www.signametrics.com**

## Extractor software supports all bus transactions

Data Extractor software can pull out transaction data on the fly; run indefinitely; capture entire test sequences; monitor embedded-system data flows during normal operation; and process or store megabytes, gigabytes, or terabytes of information. The software can collect raw data from parallel, serial, SPI, I²C, I²S, high-speed-asynchronous, full- and low-speed-USB, SMBus, one-wire, and CAN (controller-area-networks) buses. Each Data Extractor costs $495, and the Data Extractor bundle, which combines all 10 Data Extractors, costs $1995.

**CWAV, www.usbee.com**

## Controller features bar-code/ OCR-reader technology

The multichannel, microprocessing Synergy Controller features a bar-code/OCR (optical-character-recognition)-reading feature. The environmental-chamber controller's new macro capability receives the digital data from a part's bar-code/OCR label, then selects and implements the appropriate test profiles without further operator intervention. The Synergy Controller costs $2750.

**Tidal Engineering Corp, www.tidaleng.com**

## Digitizer cards offer single-ended and differential-input termination

With available sampling rates from 200k samples/sec to 3M samples/sec and two-, four-, or eight-channel configurations, the 12 digitizer cards in the UF2-4600 series use multiple 16-bit ADCs for true simultaneous sampling. The cards support single-ended and reduced-noise differential-input termination without reducing channel count. Each channel consists of an independent amplifier, which the user can program with the best voltage range to match each sensor. The ranges available are from ±10V to ±50 mV. A self-calibration feature ensures the removal of any voltage offsets before recording. The Ultrafast UF2-4600 card's prices range from $3190 for the two-channel, 200k-sample/sec UF2-4620 card to $11,990 for the eight-channel, 2M-sample/sec version.

**Strategic Test Corp, www.strategic-test.com**

## Debugging interface supports new microprocessor families

The usb2Sprite debugging interface targets Freescale Semiconductor's ColdFire and DSP 56300 microprocessor families. The device provides an embedded-system designer with a USB 2.0 interface to the on-chip-debugging features, including the vendor's GNU tools. The usb2Sprite embedded-system-debugging interface costs $225.

**Macraigor Systems, www.macraigor.com**

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**EDN BUSINESS STAFF**

**PRESIDENT, BOSTON DIVISION**
Stephen Moylan, smoylan@reedbusiness.com; 1-781-734-8431; fax: 1-781-290-3431

**PUBLISHER, EDN WORLDWIDE**
John Schirmer, jschirmer@reedbusiness.com; 1-408-345-4402; fax: 1-408-345-4400

**OFFICE MANAGER**
Rose Murphy, MurphyS@reedbusiness.com; 1-781-734-8457; fax: 1-781-290-3457

**NORTHERN CA/SILICON VALLEY**
Patti Sellman
patti.sellman@reedbusiness.com
1-408-345-4439
fax: 1-408-345-4400

**PACIFIC NORTHWEST/NORTHERN CA/ID/NV/OR/WA/WESTERN CANADA**
Judy Hayes
judy.hayes@reedbusiness.com
1-408-345-4437
fax: 1-408-345-4000

**MIDATLANTIC/MIDWEST/CENTRAL CANADA/DE/IA/IL/IN/KS/KY/MD/MI/MN/MS/MT/ND/NE/NJ/NY/OH/PA/SD/TN/WI/WV/WY**
Jim Dempsey
jim.dempsey@reedbusiness.com
1-440-333-3040
fax: 1-440-333-3044

**NEW ENGLAND/CT/GA/MA/ME/NC/NH/RI/SC/VA/VT/EASTERN CANADA (ONTARIO, QUEBEC)**
Joe McCabe
jmccabe@reedbusiness.com
1-781-734-8433
fax: 1-781-290-3433

**SOUTHWEST/SOUTHERN CA/AZ/CO/NM/UT**
Leah Vickers
ljvickers@reedbusiness.com
1-562-598-9347, fax: 1-408-345-4400

**SOUTH CENTRAL/AL/AR/FL/LA/MO/OK/TX**
Roger Buckley
rbuckley@reedbusiness.com
1-972-216-5104, fax: 1-972-216-5105

**NATIONAL SALES DIRECTOR**
Alan Robinson
aarobinson@reedbusiness.com
1-408-345-4450
fax: 1-408-345-4400

**SENIOR INTERNET SALES DIRECTOR**
Barbara Couchois
barbara.couchois@reedbusiness.com
1-781-734-8405
fax: 1-781-290-3405

**DISPLAY ADVERTISING, SUPPLEMENTS, PRODUCT MART, INFO CARDS, LIT LINK, AND RECRUITMENT**
Alan Robinson
aarobinson@reedbusiness.com
1-408-345-4450
fax: 1-408-345-4400

**WEB OPERATIONS**
Jennifer Kavanagh, Director
jkavanagh@reedbusiness.com

**ADVERTISING SERVICE COORDINATOR**
Nancy McDermott
nmcdermott@reedbusiness.com
1-781-734-8130
fax: 1-781-734-8086

**VP OF INTERNATIONAL SALES**
Mike Hancock
mike.hancock@rbp.co.uk
+44 208-652-8248
fax: +44 208-652-8249

**UK/NORWAY/SWEDEN/DENMARK/FINLAND/NETHERLANDS/BELGIUM/LUXEMBOURG**
John Waddell
jwadds@compuserve.com
+44 208-312-4696
fax: +44 208-312-1078

**AUSTRIA/GERMANY**
Adela Ploner
adela@ploner.de
+49 8131 366 99 20
fax: +49 8131 366 99 29

**ISRAEL**
Asa Talbar
talbar@inter.net.il
+972-3-5629565
fax: +972-3-5629567

**ITALY**
Roberto Laureri
media@laureriassociates.it
+39 02-236-2500
fax: +39 02-236-4411

**SWITZERLAND**
Gino Baretella
baretella@exportwerbung.ch
+41 1880-3545
fax: +41 1880-3546

**FRANCE/PORTUGAL/SPAIN**
Alain Faure
Alain.Faure@wanadoo.fr
+01 53 21 88 03
fax: +01 53 21 88 01

**JAPAN**
Toshiyuki Uematsu
t.uematsu@reedbusiness.jp
+81 3-5775-6057

**SOUTH KOREA**
Andy Kim
andy.kim@rbi-asia.com
+822 6363 3038
fax: +822 6363 3034

**SINGAPORE, MALAYSIA, THAILAND**
Chen Wai Chun
waichun.chen@rbi-asia.com
+65 6780 4533
fax: +65 6787 5550

**TAIWAN**
Charles Yang
+886 4 2322 3633
fax: +886 4 2322 3646

**AUSTRALIA**
David Kelly
david.kelly@rbi.com.au
+61 2-9422-2630
fax: +61 2-9422-8657

**HONG KONG**
Simon Lee
simonlee@rbi-asia.com.hk
+852 2965-1526
Dolf Chow
dolfchow@rbi-asia.com.hk
+852 2965-1531





**MARKETING COORDINATOR, EDN WORLDWIDE**
Tara Wietecha, tara.wietecha@reedbusiness.com
1-781-734-8450

**DIRECTOR OF CUSTOM PUBLISHING**
Cindy Fitzpatrick, cfitzpatrick@reedbusiness.com
1-781-734-8438, fax: 1-781-290-3438

**EDITORIAL/WEB PRODUCTION MANAGER**
Diane Malone, dmalone@reedbusiness.com
1-781-734-8445, fax: 1-781-290-3448

**ADMINISTRATION**
John Blanchard, Vice President of Manufacturing
Norm Graf, Creative Director
Gloria Middlebrooks, Graphic Production Director
Dorothy Buchholz, Group Production Director

**DESIGN**
Dan Guidera, Senior Art Director/Illustration

**RESEARCH DIRECTOR**
Rhonda McGee, rmcgee@reedbusiness.com
1-781-734-8264, fax: 1-781-290-3264

**CIRCULATION MANAGER**
Jeff Rovner, jrovner@reedbusiness.com
1-303-470-4477

**REED BUSINESS INFORMATION**
**Tad Smith**
Chief Executive Officer
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*November 2006*

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# scope

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## LOOKING AHEAD

### To the world's great electronics show

**That show would be Electronica, in Munich, Germany, November 14 to 17. The sheer size and audacity of the show set it apart from any other: 3000 exhibitors in a complex of halls the size of a modest town. Given its enormous scale, Electronica is not necessarily a great place to look for specifics—you might never find even the correct exhibit hall. But to understand the pervasiveness of electronics in modern life, the range of technologies involved, and the vast complexity of the supply chains that keep the industry moving, nothing can match this event.**

## LOOKING BACK

**50 YEARS AGO IN *EDN***

### Early digital logic

Timing switches control the latest automatic elevators at the new Socony Mobil Building. Thirty-two elevators in the building operate completely automatically, without operators. Each of the six banks of cars, including four service elevators, has its own master control room. Even though not signaled, the proper number of cars to handle the traffic demands of the moment are in motion at any given time during the day to cut waiting time to a minimum. The automatic control prevents cars from bunching unnecessarily at the lobby or upper floors.

Produced by Tork Clock Company, the timing switches are installed in elevator systems from the Otis Elevator Co. An important factor in the smooth-running operation of the elevators is the fact that the cars are placed "on duty" automatically during peak traffic periods, and then taken out of operation when they are not needed.

—*EDN*, October 1956

## LOOKING AROUND

### With a little concern

This month, analysts continued to ease back on their forecasts for semiconductors, end products, and capital equipment for 2006. Unofficially, some sources are saying that the inventory build-up in semiconductors, which analysts are already watching nervously, is much worse in Asia than the numbers suggest. Add to that scenario another slip-up with the PlayStation 3 and the failure of any promising next-big-thing candidate—whether it's wireless USB, digital-video broadcast, or whatever—to catch consumers' imaginations the way the original iPod did, and things could get grim. The only obvious reason for optimism is the chance—which is far from certain—that if Windows Vista actually ships to businesses in November and to consumers in January, it will trigger another wave of replacement buying in the PC arena. The new OS reportedly has the CPU, graphics hardware, and memory appetite to do just that. But will consumers adopt it quickly enough?

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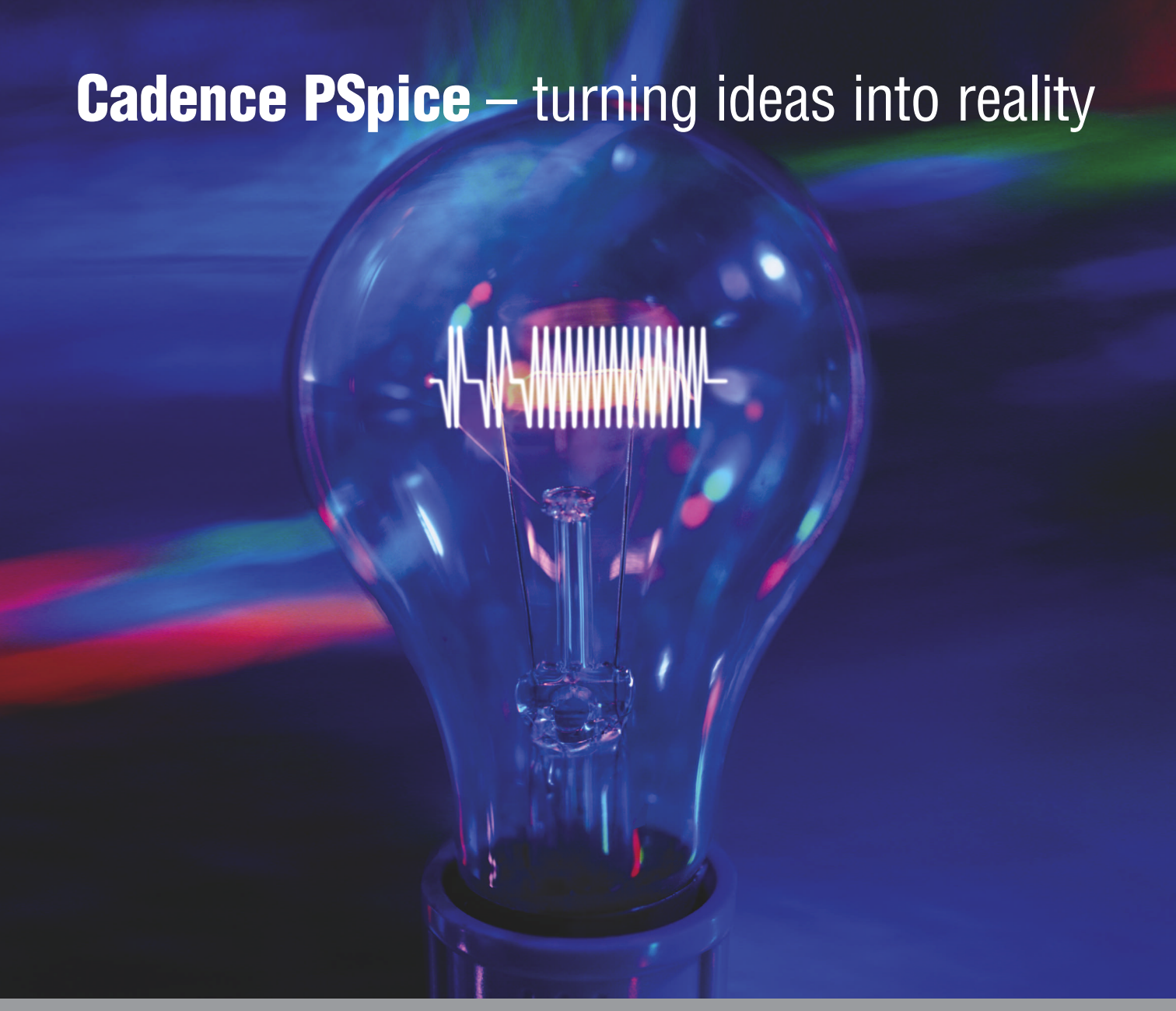

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